GRL PCIe Base Gen 3 MOI
for Tektronix 8Gbps Physical Layer Test Suite

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Revision Record

Version	Revision Date	Description of Changes	Author(s)
1.0	5/2016	GRL-PCIE3-MOI Add Software Guide. Add Advanced Features.	Bill Altmann (GRL) baltmann@graniteriverlabs.com

1 Introduction

Receiver device compliance ensures correct data detection by the receiver for an acceptable bit error ratio (BER). PCIe Base Gen-3 devices shall support a BER that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits) when a signal with valid voltage and timing characteristics are delivered to the receiver compliance point [1]. The corresponding signal properties for verifying receiver tolerance should include the maximum allowable jitter, noise and signal loss.

This document describes the step by step calibration and procedures to perform the Receiver Jitter Tolerance test as specified in the PCIe Base 3.0 Standard using the Tektronix BERTScope. The BERTScope and appropriate accessories provide the necessary test patterns with jitter, ISI, and crosstalk. Additionally, the DPP125C Digital Pre-Emphasis Processor adds the required transmitter equalization. The receiver tolerance test includes various Differential Mode Sinusoidal Interference, minimum transmitter voltage amplitude, and jitter which includes random jitter including a sinusoidal periodic jitter component that is swept across specific frequency intervals.

Once the stressed receiver tolerance test setup has been calibrated the BERTScope transmits a Modified Compliance pattern to the receiver and monitors the loopback pattern has a BER that is less than 10^{-12} with a confidence level of 95%.

2 Reference Documents

[1] PCI Express® Base Specification Rev. 3.1a December 7, 2015

[2] Tektronix PCIe Gen3 Base MOI (55w-2428589-0)

3 Resource Requirements

3.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS - SYSTEMS

Equipment	Qty.	Description	Key Specification Requirement Tektronix P.N.
BSA125C or higher	1	12.5 Gb/s BERTScope	Requires option STR for stress generation
DPO/MSO70000DX	1	Real-time oscilloscope	≥ 20 GHz bandwidth
DPP125C or DPP125B	1	Digital Pre-Emphasis Processor	
CR125A or higher	1	12.5 Gb/s Clock Recovery Unit	Used for DUT-sourced reference clock applications. Not required for BERT-sourced reference.
Artek A2	1	ISI Generator	Programmable ISI Generator (optional)
AFG3000	1	Arbitrary Function Generator	120MHz Sine Wave Generator
Combiner	1	Combine Differential Mode (DMI) and AC Common Mode with stressed Rx test pattern.	
Seasim Application from PCI-SIG	1	Simulation Software of Eye Opening at TP2P	

TABLE 2. EQUIPMENT REQUIREMENTS - CABLES

Equipment	Qty.	Key Specification Requirement Tektronix P.N.
T+M SF104PE/11PC35/11PC35/500mm	3	174-6663-00
T+M SF104PE/11PC35/11PC35/1000mm	2	PMCABLE1M
T+M MF141/16SMA/16SMA/200mm	3	174-6664-00
T+M MF141/16SMA/16SMA/300mm	1	174-6665-00
T+M MF141/16SMA/16SMA/500mm	1	174-6666-00
T+M MF141/11SMA/16SMA/1.829M	2	174-6667-00

3.2 Software Requirements

See Table 1.

4 Calibration

PCIe calibration will be done at 3 test points: TP1 and TP2 and TP2P. TP1 is a physical test point for calibration without the effect of breakout channel length. TP2, is test point that will affect the eye opening due to trace length. TP2P, is an test point calculated by software tool ***Seasim*** to simulate the eye opening after applying Rx Behavioral package, Rx CTLE, DFE (if required).

4.1 Calibration Process Connection Setups

4.1.1 Calibration for TP1

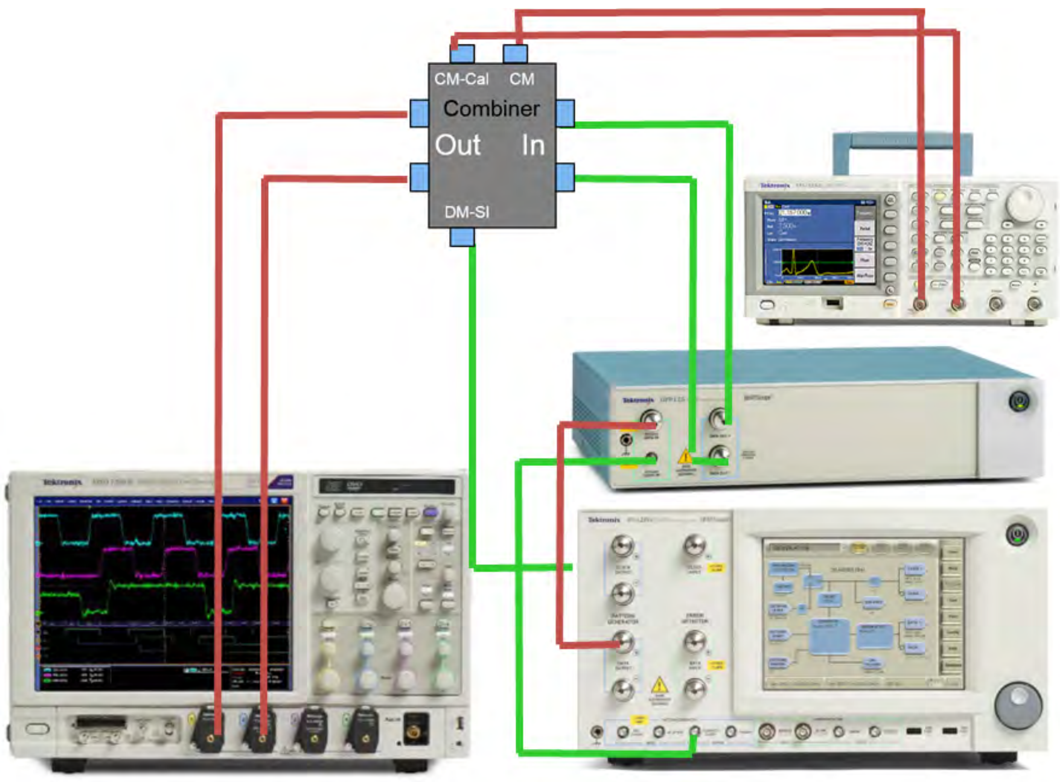


FIGURE 1. TYPICAL SETUP FOR TP1 CALIBRATION

Connection Steps:

1. Connect BERTScope Data(+) to DPP.
2. Connect BERTScope Clk Out to DPP.
3. Connect DPP Data(+) out to Combiner In.
4. Connect DPP Data(-) out to Combiner In.
5. Connect AFG Output1 to Combiner CM-IN.
6. Connect BERTScope (real panel) SI-out to Combiner DM In.
7. Connect Combiner Data Out to Tek Scope Chan1 and Chan2.

4.1.2 Calibration for TP2

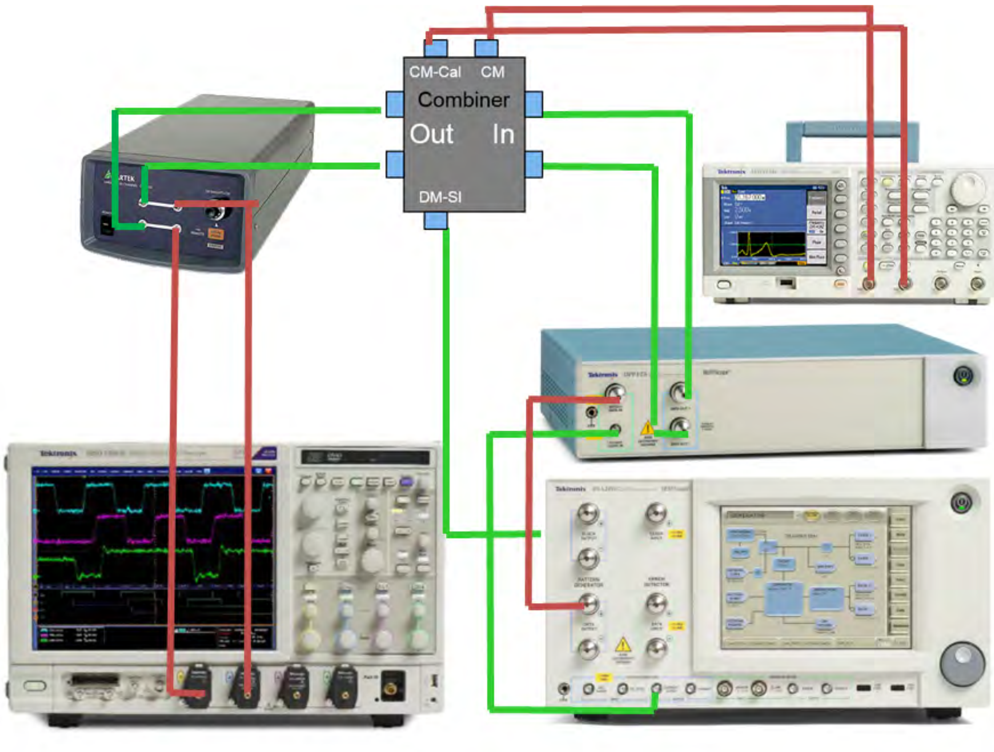


FIGURE 2. TYPICAL SETUP FOR TP2 CALIBRATION

Connection Steps:

1. Connect BERTScope Data(+) to DPP
2. Connect BERTScope Clk Out to DPP
3. Connect DPP Data(+) out to Combiner In
4. Connect DPP Data(-) out to Combiner In
5. Connect AFG Output1 to Combiner CM-IN
6. Connect BERTScope (real panel) SI-out to Combiner DM In
7. Connect Combiner Data Out to Artek ISI Box Input
8. Outputs of Artek ISI Box connect Tek Scope Chan1 and Chan2

5 Software

5.1 Setup

This section provides procedures for installing, configuring, and verifying the operation of the GRL PCIe Base 3.0 Rx Test solution. It also will help you familiarize yourself with the basic operation of the application.

The software installer automatically creates short cuts in the Desktop and Start Menu.

To open the application, follow the procedure in the following section.

5.1.1 Launch and Setup Software

5.1.1.1 On the BERTScope

1. Select View > System > Tools Tab.
2. Under Utilities Column, press the Remote button.
3. In Remote Window, Select TCP/IP.
4. Change Terminator to "LF". Press the Connect Button. See Figure 3.
   a) If you see an error pop-up when pressing the Connect button. Try a different Port. For example, change Port 23 to 21.
5. Address and Port # on Remote Client. It will be needed to connect BERTScope to automation software.
6. Minimize, but do not close, the *Remote Client* Window.

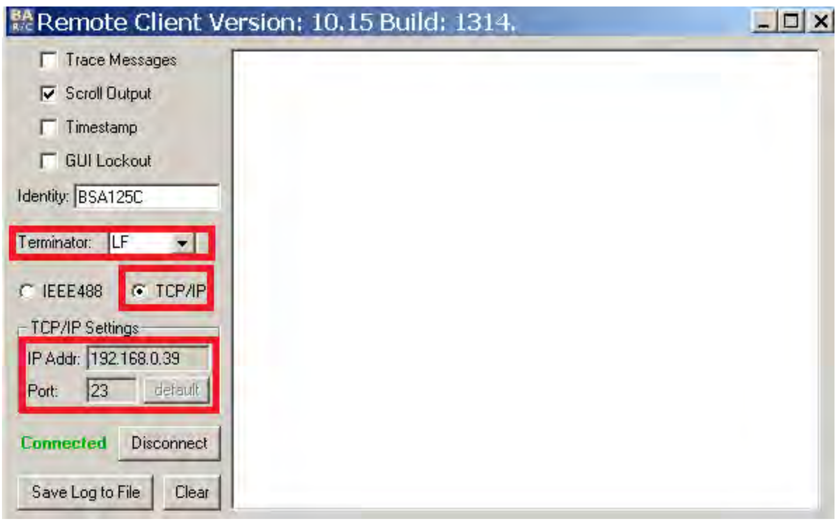


FIGURE 3. REMOTE CLIENT WINDOW

5.1.1.2 On the PC Used for GRL Framework Installation.

1. Navigate to Start Menu > All Programs > GRL > GRL Automated Test Solutions.

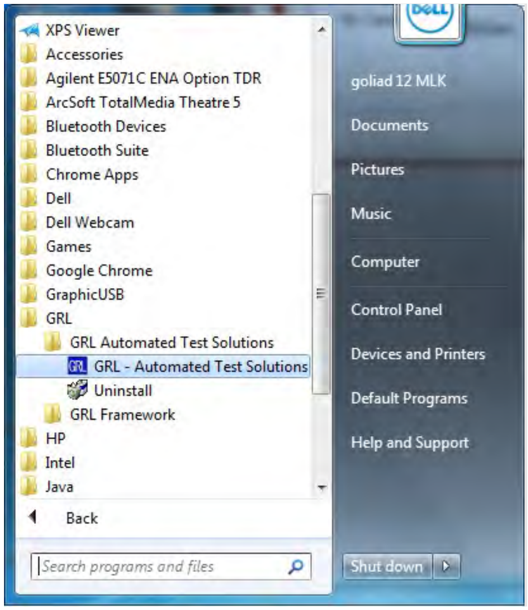


FIGURE 4. GRL AUTOMATED TEST SOLUTIONS IN START MENU

2. Click Application>Rx Test Solution>PCIe 3.0 Base Rx Test to open the application.

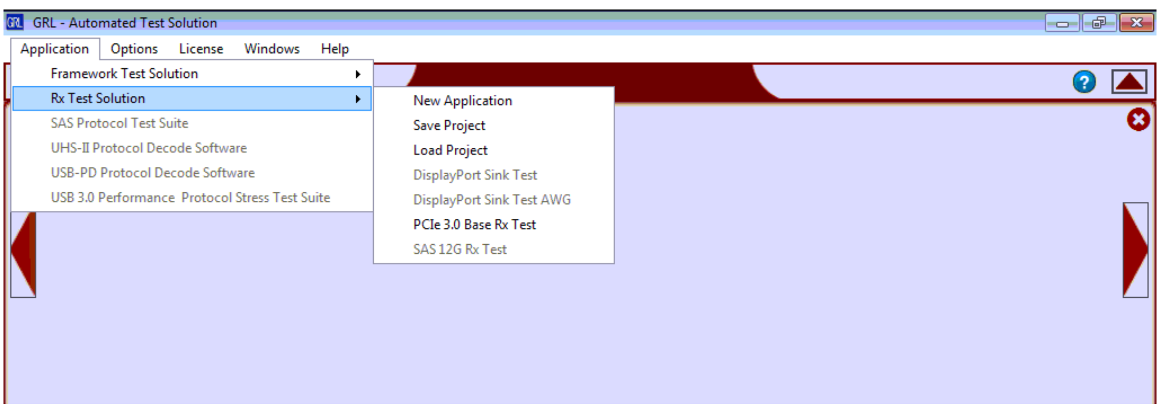


FIGURE 5. RX TEST SOLUTIONS IN GRL AUTOMATED TEST SOLUTIONS WINDOW

3. To enable license, go to License->License Details. The dialog in Figure 6 will pop up.

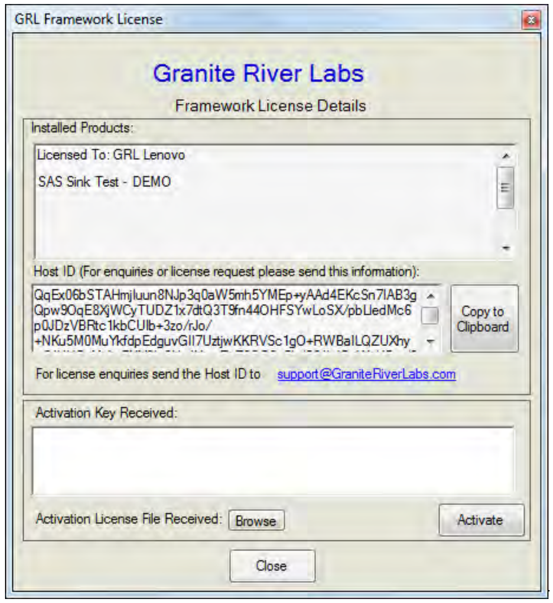
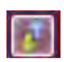


FIGURE 6. LICENSE DETAILS WINDOW

4. Activate License:

   a) If you have an Activation Key, please enter in the box provided and press **Activate**.
   b) If you do not have an Activation Key, press **Close** to use the SW for 10 Days free of charge.

   Note: Once the 10-day trial times out, you will need to request an activation key for future usage on the same computer or oscilloscope. The demo SW is also limited in its capability in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request a License key by contacting support@graniteriverlabs.com.

5. Click on Equipment Setup icon  on the GRL Framework.
6. Enter the BERTScope IP address and Port number to match what is in the BERTScope *Remote Client* window shown in Step 4-5.
7. Attach Tek AFG via USB to TekScope / Connect with LAN.

8. On Tek Scope, open the application **OpenChoice Instrument Manager**. See Figure 7.

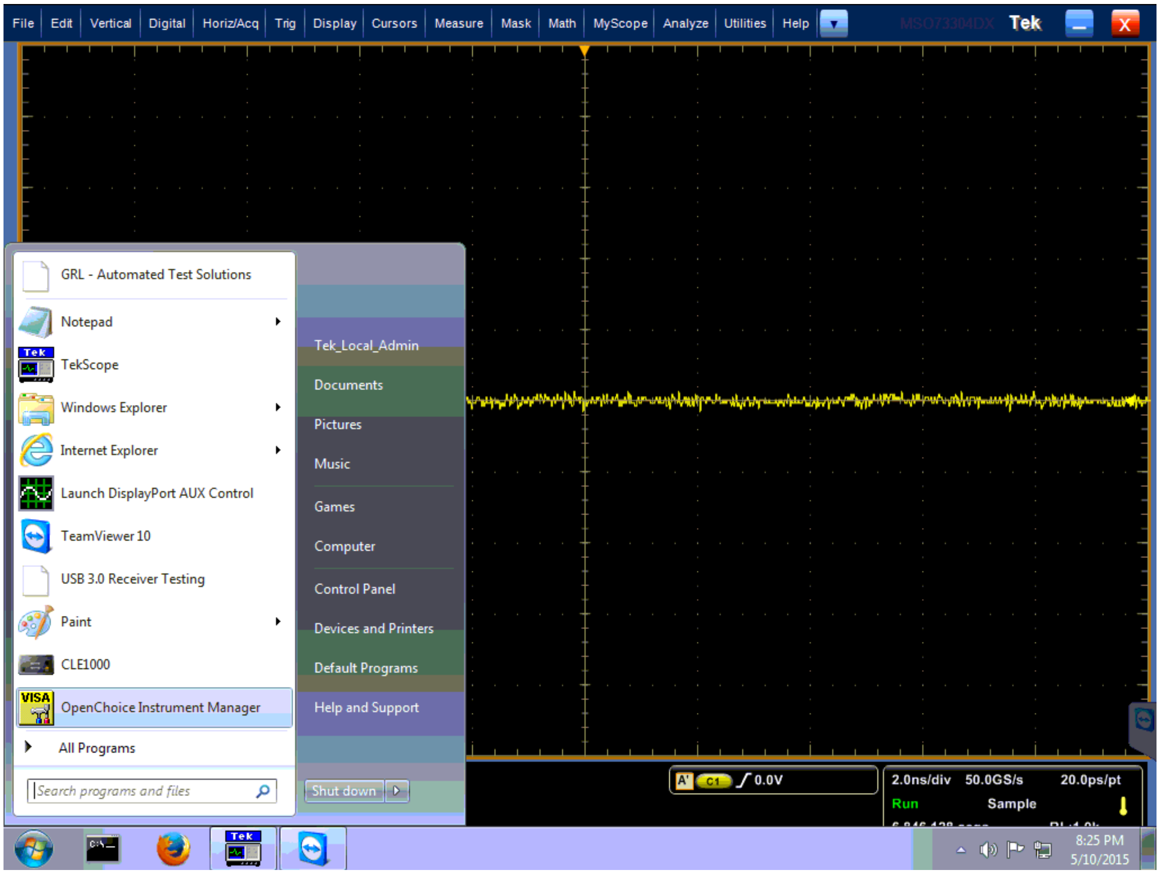


FIGURE 7. OPENCHOICE INSTRUMENT MANAGER IN START MENU

9. Instrument Manager will display all the connected instruments on its list, as in Figure 8:

   a) GPIB8::1::INST (Tek Scope)
   b) TCPIP::192.168.0.39::23::SOCKET (BertScope)
   c) USB:: 0x0699::0x0345::C022203::INSTR (AFG)

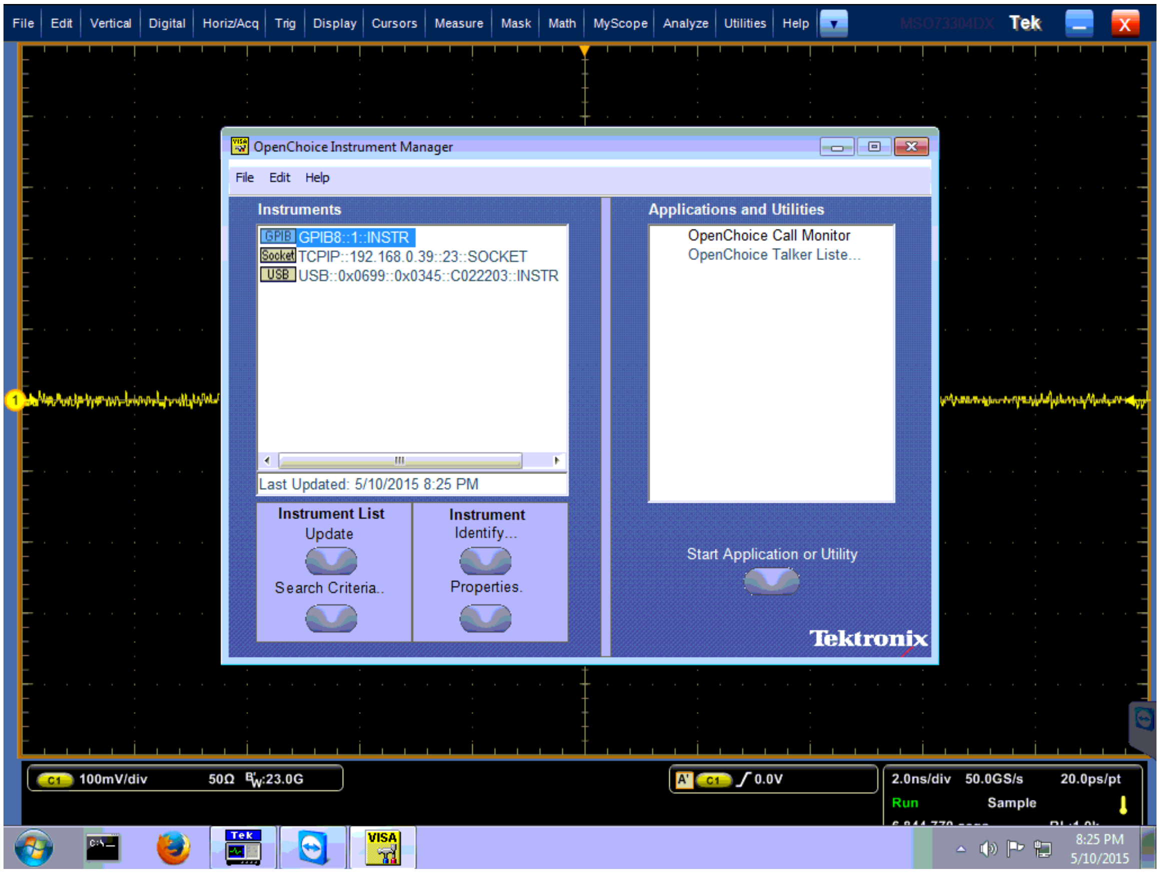


FIGURE 8. INSTRUMENT LIST IN INSTRUMENT MANAGER

10. Note these settings, as in Figure 9 and Figure 10:

   a) Enter the Scope IP Address.
   b) Enter BertScope IP Address.
   c) Enter Tektronix AFG USB/IP Address.
   d) Enter the COM Address of the ISI Generator to be used.

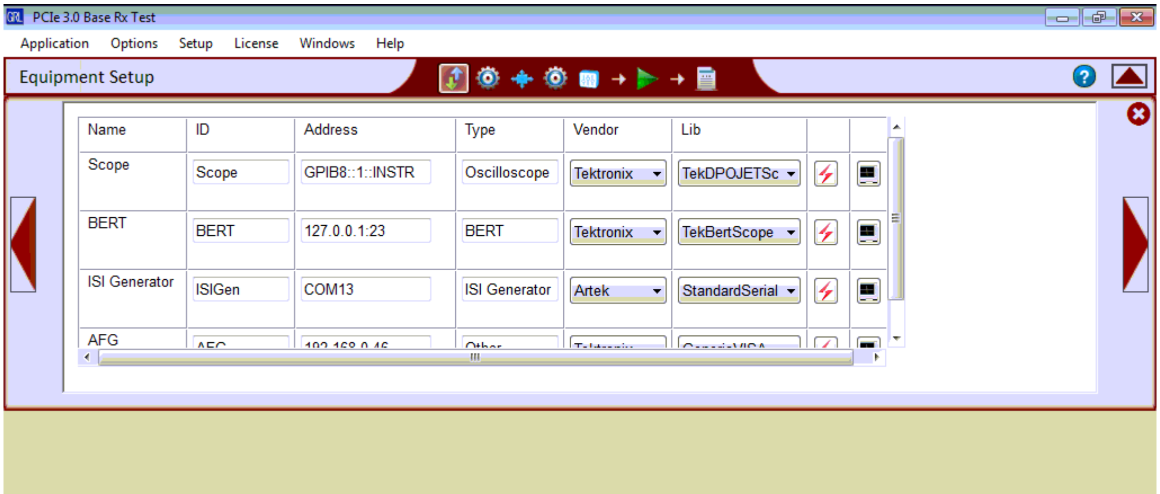


FIGURE 9. EQUIPMENT SETUP WINDOW – VIEW #1

FIGURE 10. EQUIPMENT SETUP WINDOW – VIEW #2

11. Check the connection by pressing the “lightning” button . The “lightning” button should turn green if the connection has been verified.
12. Do this for each instrument that that will be used, as shown in Figure 11.

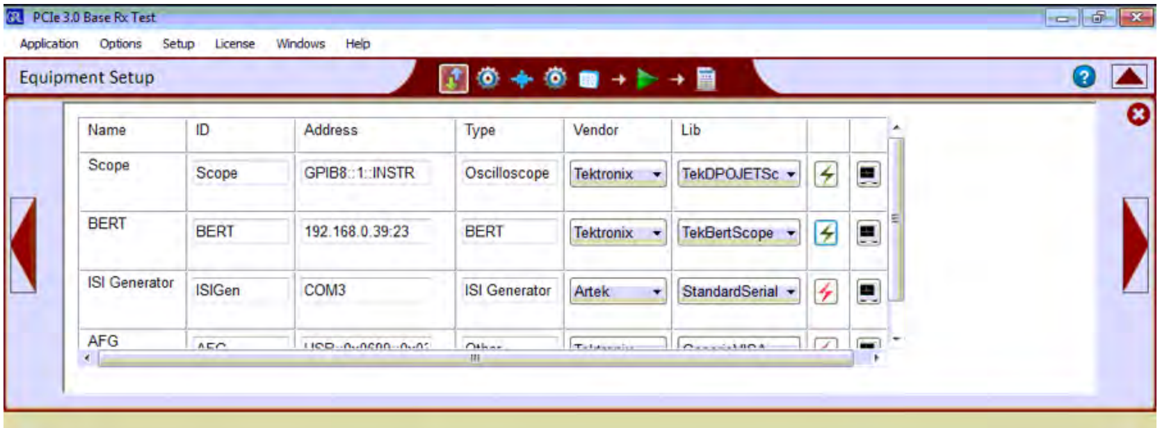


FIGURE 11. EQUIPMENT SETUP WINDOW – VIEW #3

5.1.2 Additional Notes

The USB driver SW for the ISI Generator being used must be installed on the PC being used for testing and the ISI Generator must be connected to the PC via USB. The driver for the ISI Generator is available from the ISI Generator manufacturer. Refer to Appendix of this document for driver installation information for supported ISI generators.

5.2 Calibrating Using the Software

5.2.1 Session Info

The information provided will be included in the report.

The **DUT Information and Test Info** are input by the user.

The **SW Versions** information is automatically populated.

FIGURE 12. SESSION INFO

5.2.2 Conditions for Testing and Calibration

In this section, conditions for Testing and Calibration will need to be set. User selects conditions for testing and for calibration. 

When calibrating, the application will calibrate the selected range, Sj frequency, common mode voltage and differential voltage that the user chooses.

Recommended procedure:

1. When calibrating, select conditions for calibration and perform desired calibration
2. When testing: re-select desired conditions for testing. For example, it may be only necessary to test range A at Sj frequency. The user would select the appropriate conditions for test

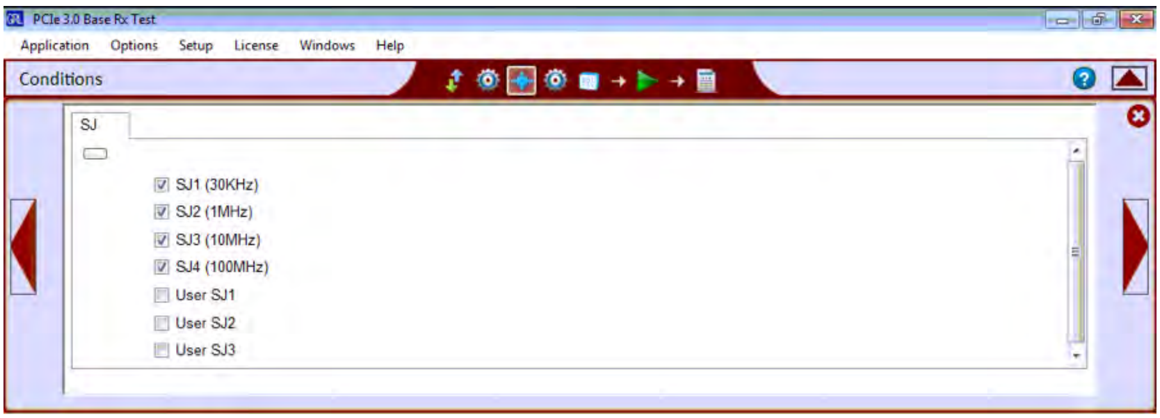


FIGURE 13. CONDITIONS FOR TESTING AND CALIBRATION

5.2.3 Setup Configuration

5.2.3.1 ISI Generator Setup

If test is running using BERTScope ISI Trace board (For more information on how to generate desired insertion loss using BERTScope ISI Trace board, please refer to Appendix B), user can set the ISI to NONE.

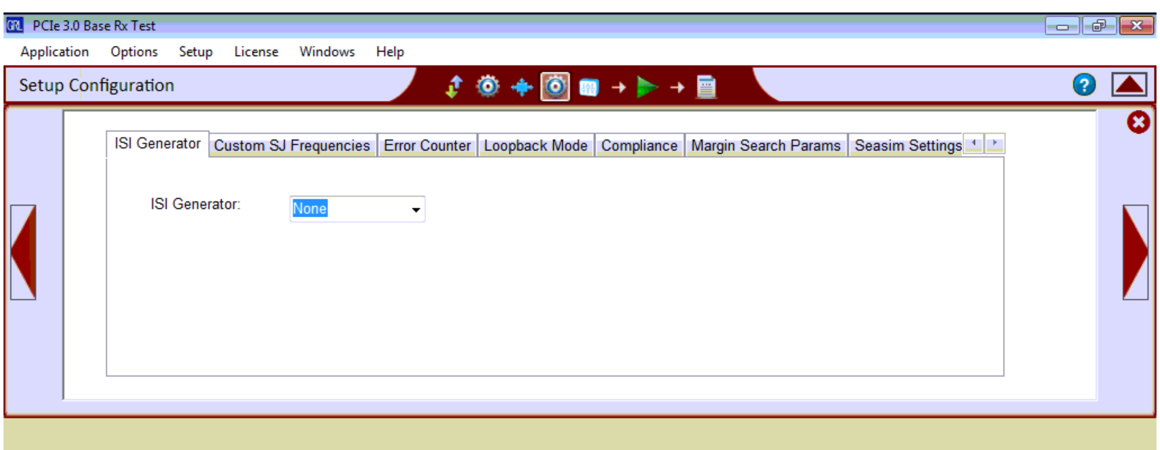


FIGURE 14. ISI GENERATOR SETUP

5.2.3.2 Custom SJ Frequency

Set Custom SJ frequency to test for condition setup on previous tab.

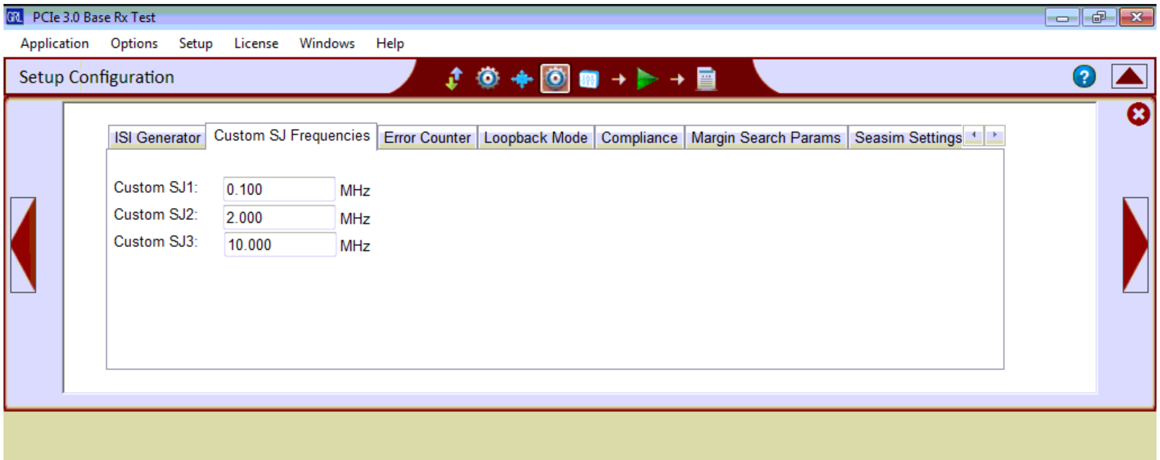


FIGURE 15. CUSTOM SJ FREQUENCIES

5.2.3.3 Error Counter

Select Receiver base DUT loop back capability. If DUT can be configured to loop back mode, select Loopback, else select Manual.

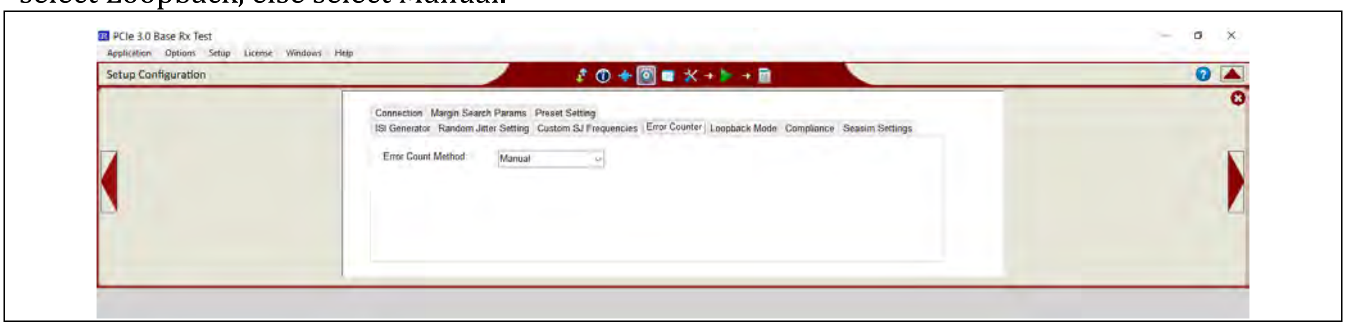


FIGURE 16. ERROR COUNTER SETUP

Details on the use of Manual mode will be provided in a future version of this document.

5.2.3.4 Loopback Mode

If the user selected loopback on the Error Counter tab, then the user needs to select "Clock Recovery" in the Clock Recovery Method drop-down on the Loopback Mode tab. *Other options on the Clock Recovery Method drop-down are not yet supported.*

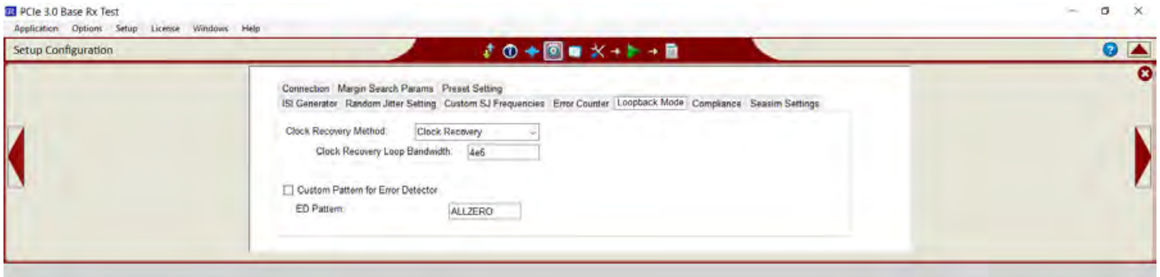


FIGURE 17. LOOPBACK MODE SETUP

PCIE uses the default pattern.

Details on the use of Custom Patterns will be provided in a future version of this document.

5.2.3.5 Compliance Tab

Set BER and Maximum Error allowed for testing. These limits are set by the Specification. Other limits may be set in these fields by the user. The syntax '1e-12' indicates 10^{-12}, and is the only syntax supported in this field.

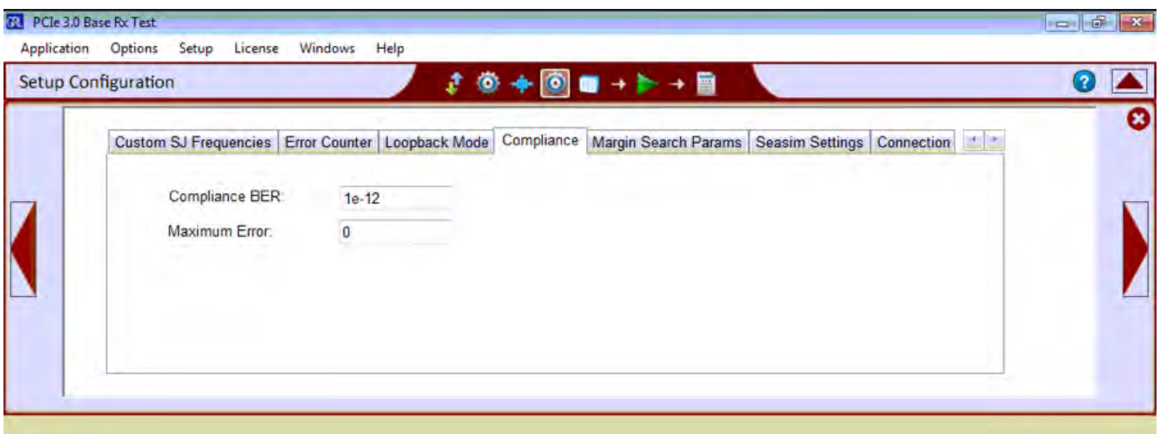


FIGURE 18. BER AND MAXIMUM ERRORS

5.2.3.6 Seasim Tab

Set if user wishes to use the Rx Behavioral package during Eye Height and Eye Width Calibration. Also set the intrinsic jitter (if required) to be used in the Seasim calculation.

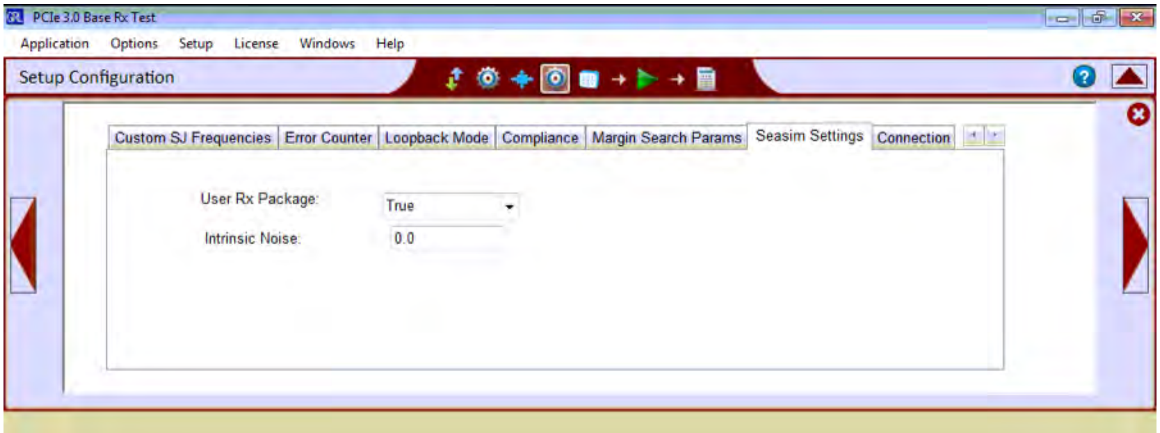


FIGURE 19. SEASIM SETUP

Details on the use of 'False' in the User Rx Package field will be provided in a future version of this document

5.2.3.7 Connection Tab

Setup connection of Data+ and Data- in Scope. Scope channels shall be assigned according to how the scope cables are attached to the test setup.

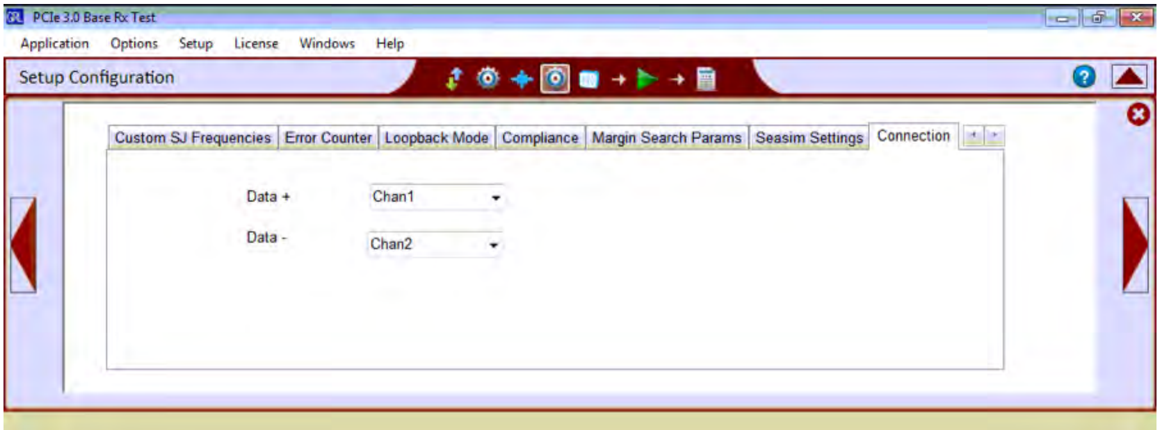


FIGURE 20. CONNECTION SETUP

5.2.4 Selecting Calibration Steps Using the Software

The **Select Calibration Tests** page is the place where the calibration tests that need to be performed are selected. Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the RX Tests will show an error message.

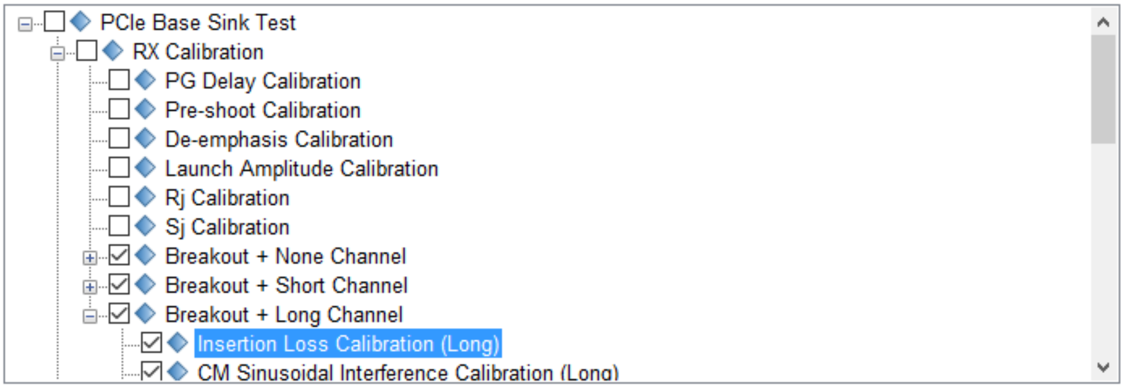
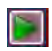


FIGURE 21. SELECT CALIBRATION TESTS PAGE

5.2.5 Run Calibration Steps

From the pop-up menu, select the Run icon: 

Skip Test if Results Exist. If previous calibration results exist, then software will *skip* calibration steps that have existing reports.

Replace if Results Exist. If previous calibration results exist, then software will replace each step in calibration with new results.

(Restart) Delete Existing Results. All previous results will be deleted, and each selected step in calibration will generate new report.

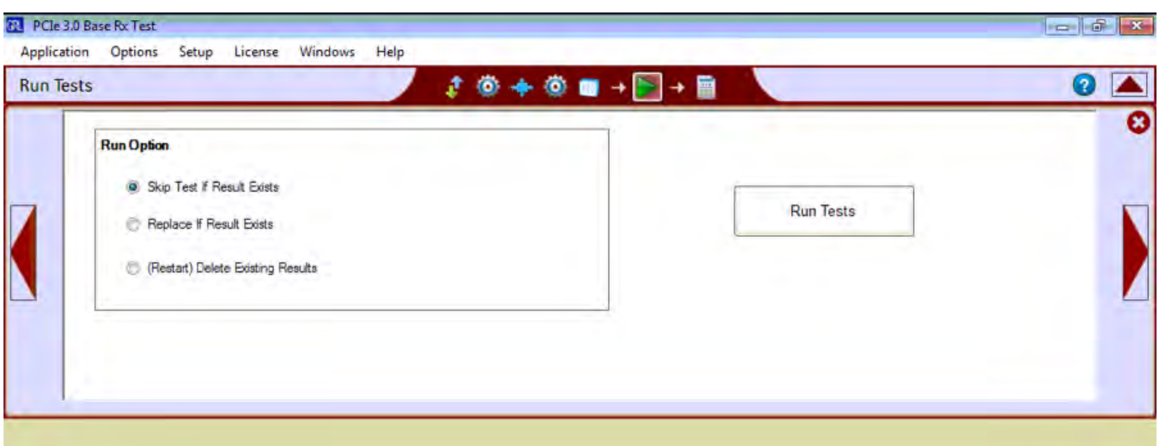


FIGURE 22. CONNECTION SETUP

5.3 Testing using GRL-PCIE3-BASE-RX Software

5.3.1 Receiver Compliance Tests

The **Select Tests** page is the place where the compliance tests that need to be performed are selected.

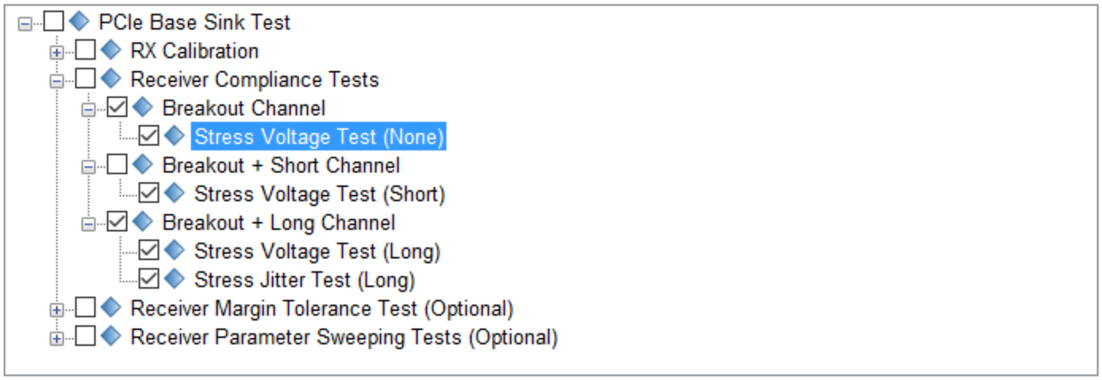


FIGURE 23. SELECT COMPLIANCE TESTS PAGE

Tests are run from the same screen as shown in Section 5.2.5.

5.3.2 Receiver Margin Tests

The **Select Tests** page is the place where the compliance tests that need to be performed are selected.

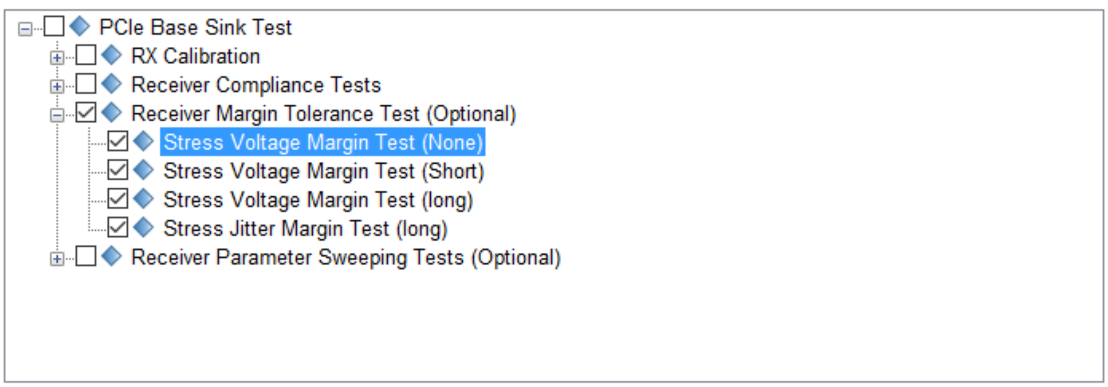


FIGURE 24. SELECT MARGIN TESTS PAGE

Tests are run from the same screen as shown in Section 5.2.5.

5.4 Report

The **Report** page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the Delete button. Also for a pdf report, click the Generate Report button. To have the calibration data plotted in the report, make sure the Plot Calibration Data box is checked.

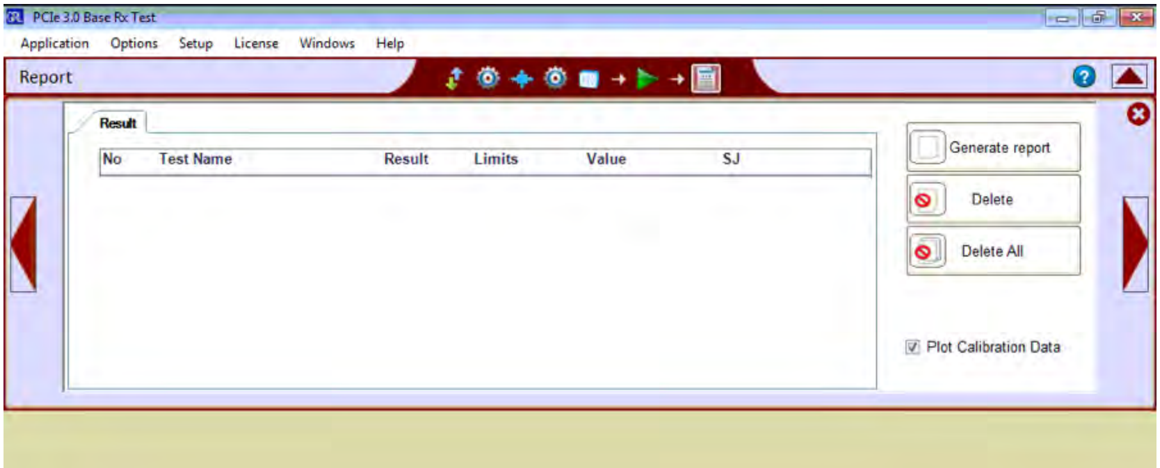


FIGURE 25. REPORT RESULTS PAGE

5.5 Interpreting a Report

5.5.1 DUT Information

This portion is populated from the information in the DUT tab from the **Session Info** tab.

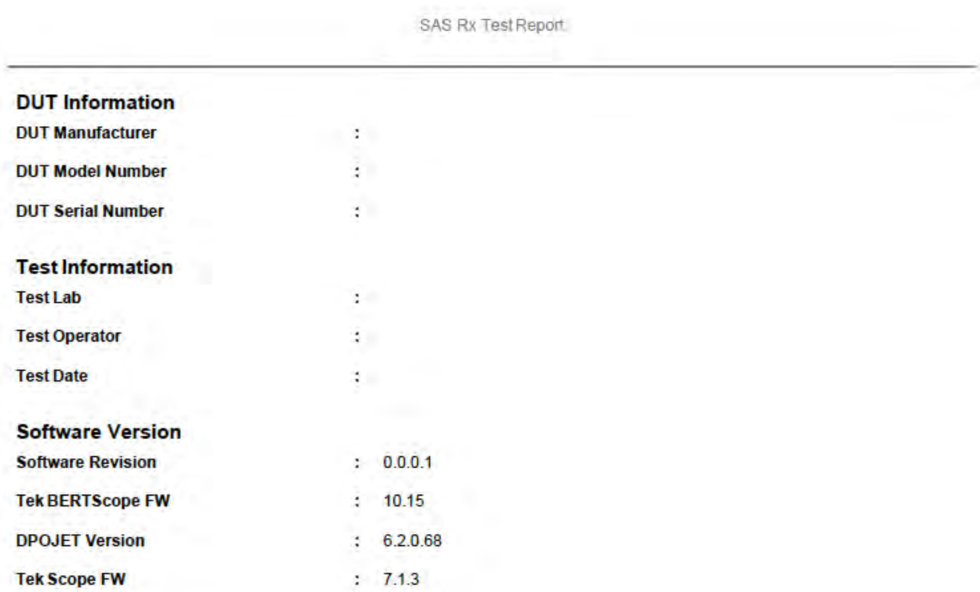


FIGURE 26. DUT INFORMATION

5.5.2 Summary Table

This portion is populated from the tests performed and its results. This gives an overall view of all the results and its test conditions.

No	TestName	Limits	Value	Results	De-Emphasis	Voltge Swing	SJ
1	Pre-shoot Calibration	True/False	True	Pass			
2	De-emphasis Calibration	True/False	True	Pass			
3	Launch Amplitude Calibration	True/False	True	Pass			
4	Rj Calibration	True/False	True	Pass			
5	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_1
6	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_2
7	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_3
8	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_4
9	CM Sinusoidal Interference Calibration (Short)	True/False	True	Pass			
10	DM Sinusoidal Interference Calibration (Short)	True/False	True	Pass			
11	Stressed Voltage Calibration (Short)	True/False	False	Fail			
12	CM Sinusoidal Interference Calibration (Long)	True/False	True	Pass			
13	DM Sinusoidal Interference Calibration (Long)	True/False	True	Pass			
14	Stressed Voltage Calibration (Long)	True/False	False	Fail			
15	Stress Jitter Calibration (Long)	True/False	False	Fail			
16	Insertion Loss Calibration (Long)	True/False	True	Pass			
17	Insertion Loss Calibration (Short)	True/False	True	Pass			
18	Insertion Loss Calibration	True/False	False	Fail			

FIGURE 27. SUMMARY TABLE

5.5.3 Calibration Data Results

If Plot Calibration Data checkbox is checked, then the plots are shown in this part of the report.

1. Pre-shoot Calibration

Test Limits	:	True/False
Result	:	True
Cal Parameter	:	PreShoot

PreShootCalibration Plot

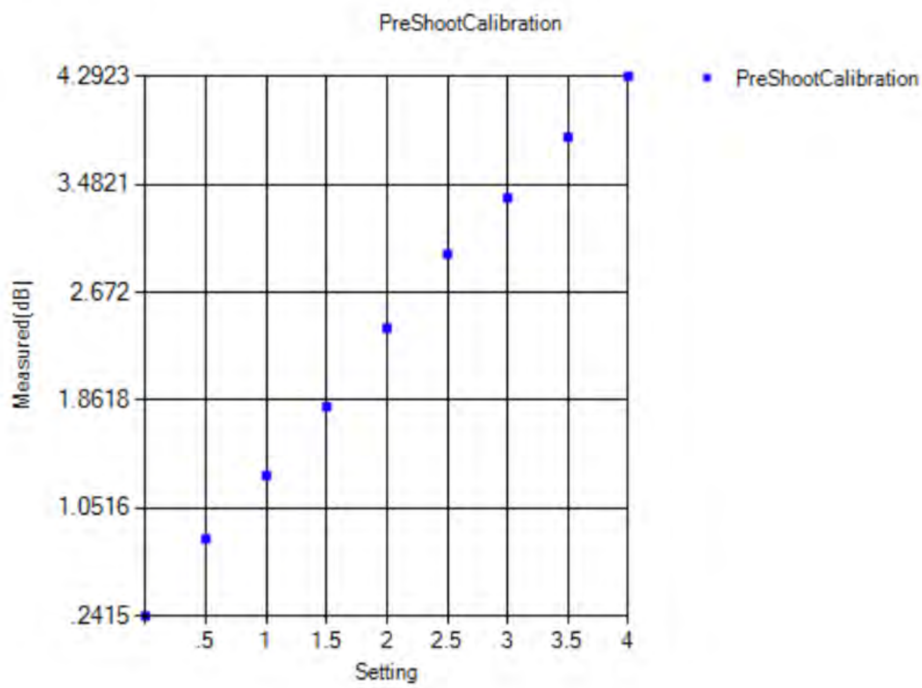


FIGURE 28. CALIBRATION RESULTS EXAMPLE

5.5.4 Compliance Test Results

PCIe 3.0 Base Rx Test Report

No	TestName	Limits	Value	Results	SJ
1	PG Delay Calibration	True/False	True	Pass	
2	Sj Calibration	True/False	True	Pass	User_SJ1
3	Sj Calibration	True/False	True	Pass	User_SJ2
4	Sj Calibration	True/False	True	Pass	User_SJ3
5	Stress Jitter Sweep Test (Long)	True/False	False	Fail	
6	Stress Jitter Test (Long)	True/False	False	Fail	SJLF_2
7	Stress Jitter Test (Long)	True/False	True	Pass	SJLF_4
8	Stress Jitter Test (Long)	True/False	True	Pass	User_SJ1
9	Stress Jitter Test (Long)	True/False	True	Pass	User_SJ3
10	Insertion Loss Calibration (Long)	True/False	True	Pass	
11	CM Sinusoidal Interference Calibration (Long)	True/False	True	Pass	
12	DM Sinusoidal Interference Calibration (Long)	True/False	True	Pass	
13	Stressed Voltage Calibration (Long)	True/False	True	Pass	
14	Stress Jitter Calibration (Long)	True/False	True	Pass	
15	Sj Calibration	True/False	True	Pass	User_SJ4
16	Sj Calibration	True/False	True	Pass	User_SJ5
17	Stress Voltage Test (Long)	True/False	True	Pass	
18	Stress Jitter Test (Long)	True/False	False	Fail	SJLF_3
19	Stress Jitter Test (Long)	True/False	True	Pass	User_SJ2
20	Stress Jitter Sweep Test (Long)	True/False	True	Pass	SJLF_3
21	Stress Jitter Sweep Test (Long)	True/False	True	Pass	SJLF_2
22	Stress Jitter Sweep Test (Long)	True/False	True	Pass	User_SJ2
23	Stress Jitter Margin Test (long)	True/False	True	Pass	User_SJ3
24	Stress Voltage Margin Test (long)	True/False	False	Fail	
25	Stress Jitter Margin Test (long)	True/False	True	Pass	User_SJ2
26	Pre-shoot Calibration	True/False	True	Pass	
27	De-emphasis Calibration	True/False	True	Pass	
28	Launch Amplitude Calibration	True/False	True	Pass	
29	Rj Calibration	True/False	True	Pass	
30	Sj Calibration	True/False	True	Pass	SJLF_1
31	Sj Calibration	True/False	True	Pass	SJLF_2
32	Sj Calibration	True/False	True	Pass	SJLF_3
33	Sj Calibration	True/False	True	Pass	SJLF_4
34	Insertion Loss Calibration	True/False	True	Pass	

FIGURE 29. CALIBRATION RESULTS EXAMPLE

5.5.5 Jitter Margin Results

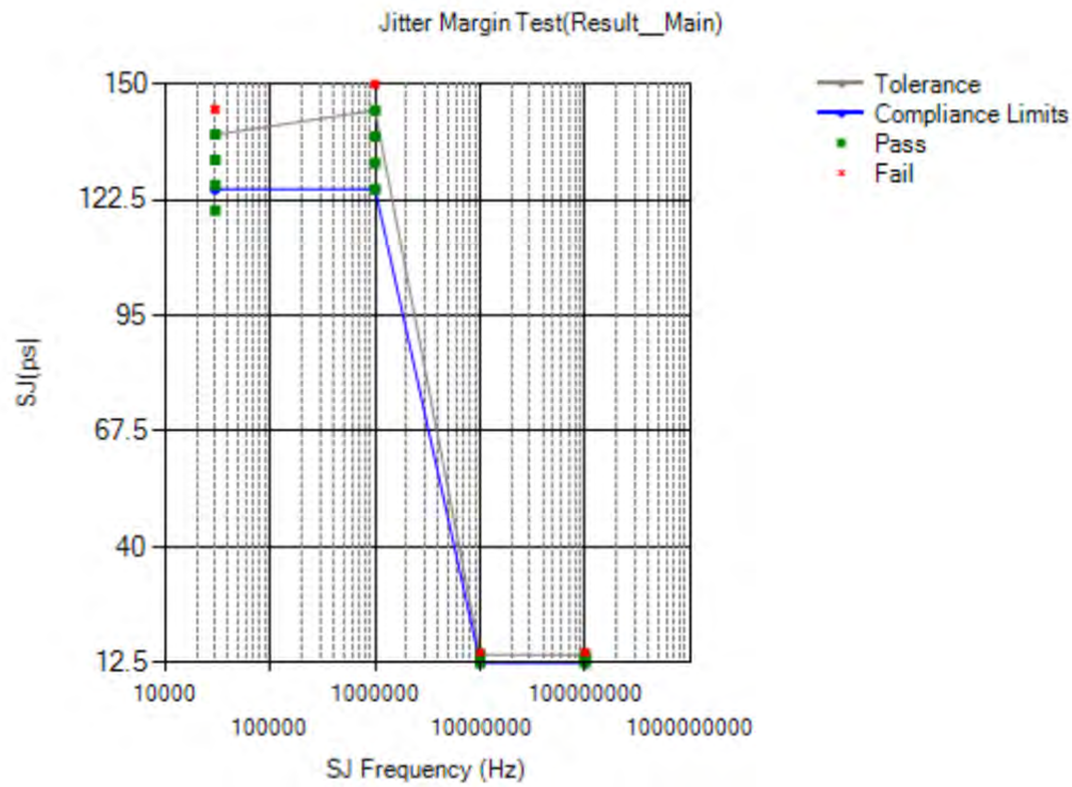


FIGURE 30. JITTER MARGIN REPORT EXAMPLE

6 Test Suite

The PCIE3 Base Specification tests are listed in the drop-down menus in the equipment described in this MOI.

7 Appendix A: ARTEK CLE1000-A2 Installation

7.1 ISI Generator Driver Installation

If using ARTEK CLE1000-A2 for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the *DP Configuration Utility*.

1. Connect the CLE1000-A2 to the PC being used as the controller, using a USB 2.0 cable.
2. Turn on the front panel power switch on the CLE1000-A2.
3. Right Click on My Computer > Manage > Device Manager. If no SW for the CLE1000-A2 has been installed, you will see a 'bang' in the device manager. See Figure 31.

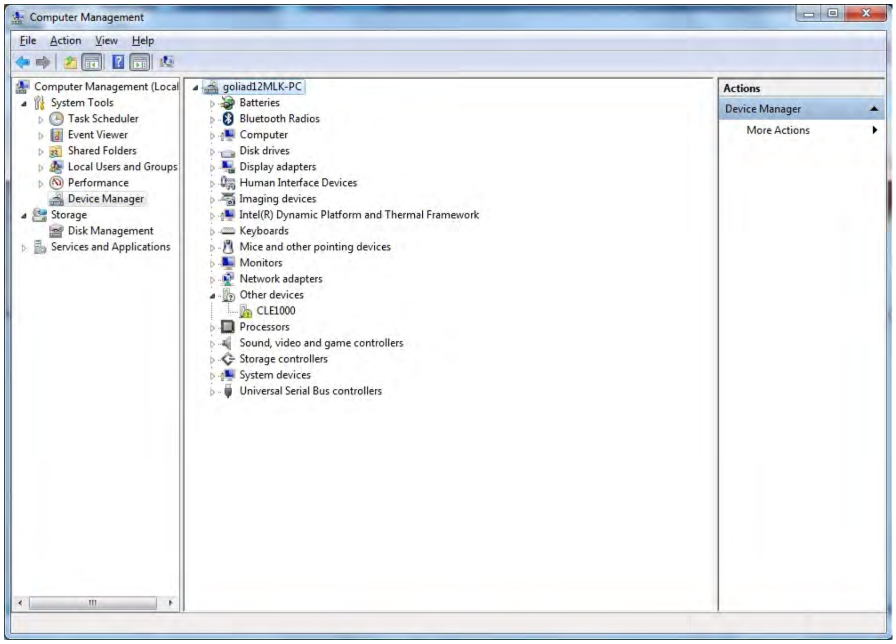


FIGURE 31. DEVICE MANAGER WINDOW

4. To install the CLE1000-A2, go to http://www.aceunitech.com/support.html and download the Control SW package for the CLE1000.
5. Unpack the CLE1000 SW .zip file.
6. Install the CLE1000 Driver:

   a) In Device Manager, right click on **CLE1000** > **Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 32.
   c) Browse to the root directory of the unzipped CLE1000 SW folder.
   d) Press Next. You will be asked to confirm your request to install a driver.
   e) Press **Install**. Driver SW will complete installation.

7. Once Installation completes, the Device Manager should look like Figure 34.

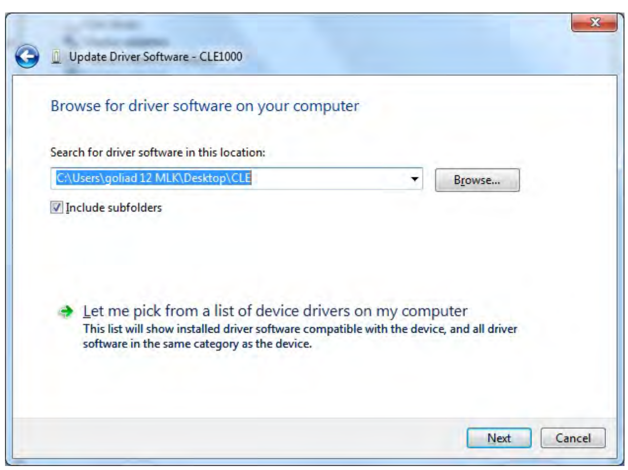


FIGURE 32. UPDATE DRIVER WINDOW

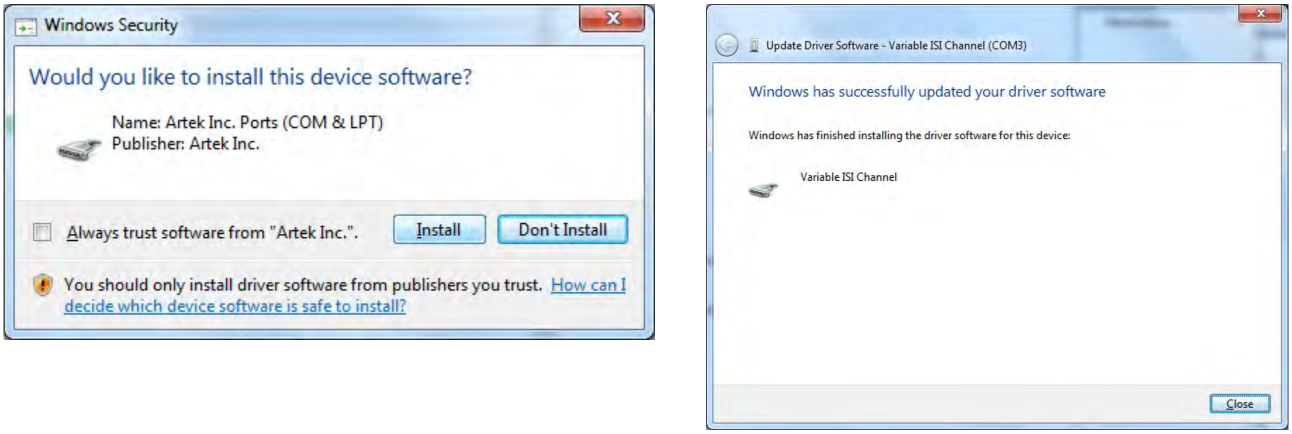


FIGURE 33. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW

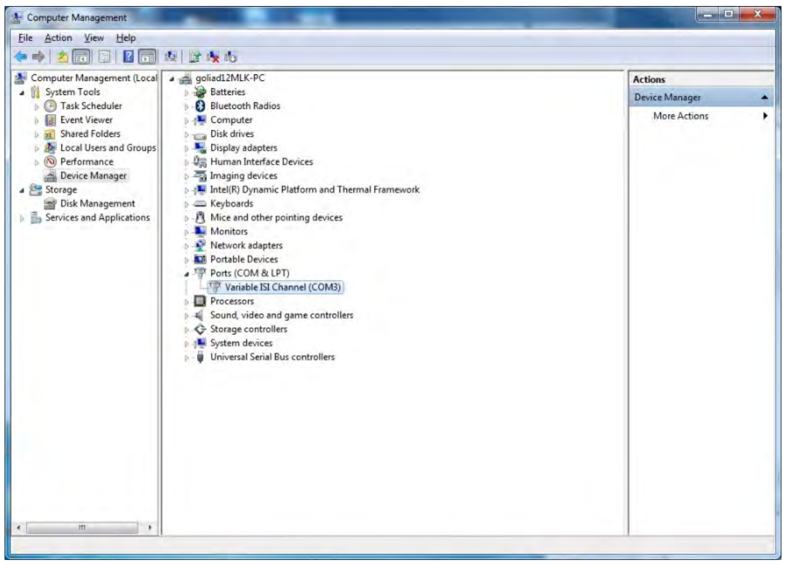


FIGURE 34. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE10000 SW driver is now installed and the CLE1000 can now be selected for use remotely using the GRL *DP Configuration Utility*.

7.2 CLE1000 GUI Installation

It may also be useful to install the CLE1000 GUI, so that the ISI channel can also be controlled manually from the PC. To install the SW, do the following:

1. In the CLE1000 SW folder, click on the Setup.exe file. Once installed successfully, the following GUI will appear on the desktop.
2. You can now close the GUI if you don't want to have manual control.

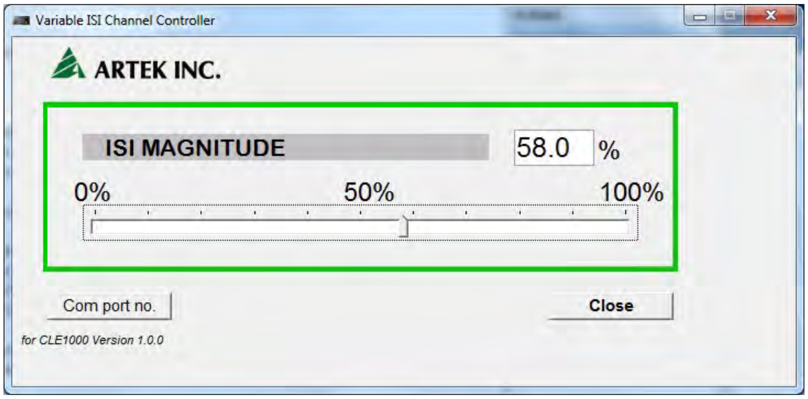


FIGURE 35. CLE1000 GUI

8 Appendix B: BERT Scope ISI Trace Board

The BERTScope ISI Trace Board is required for PCIe Base 3.0 Insertion Loss tests.

Figure 36 describes the insertion loss at 4GHz on various trace lengths on the BERTScope ISI Trace Board.

	2.42 inch	5 inch	6.75 inch	9 inch	12 inch	17 inch	24 inch	31 inch	40 inch
FREQ MHz	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB
4000	-0.89	-1.73	-2.34	-2.99	-3.9	-5.49	-7.63	-9.7	-12.54

FIGURE 36. INSERTION LOSS PER TRACE LENGTH

For PCIe Gen3. 3 Type of trace length to be tested, follow the table in Figure 37 to connect points of trace board to get the desired insertion loss.

	Target Insertion Loss(I.L.)	Trace Length(Insertion Loss)
Replica Channel	-2.5 +/- 1dB	6.75 inch (-2.34dB) Total I.L. = -2.34dB
Replica Channel + Short Channel	-12.0 +/- 2dB	6.75 inch (-2.34dB) 31 inch (-9.7 dB) Total I.L. = -12.04 dB
Replica Channel + Long Channel	-20 +/- 2dB	6.75 inch (-2.34dB) 17inch (-5.49 dB) 40 inch (-12.54 dB) Total I.L. = -20.46 dB

FIGURE 37. INSERTION LOSS CONNECTIONS TABLE

9 Appendix C: Manual Test Methods

9.1 Waveform Tests

9.1.1 Preshoot and Deemphasis

PCIe Base uses two presets for different trace lengths of the breakout board. Both Deemphasis and Preshoot are calibrated for the target dB for each preset. See Table 3.

TABLE 3. PRESETS FOR WAVEFORM TESTS

Preset	Preshoot	Deemphasis
4	0.0dB	3.5dB
7	0.0dB	-6.0dB

9.1.1.1 BERTScope Setup

1. Set the BERTScope to defaults.
2. Set Generator to 8Gpbs (PCIe Gen3 Speed)
3. Disable All stressed jitter component (Rj, Sj etc)
4. Set the Output amplitude to 800mV
5. Set the DPP Output 460mV
6. Default the DPP to 0.0dB Preshoot and Deemphasis, as shown in Figure 38.
7. Load with 64 ONEs , 64 ZEROs and 128 Clk Pattern to BERTScope.

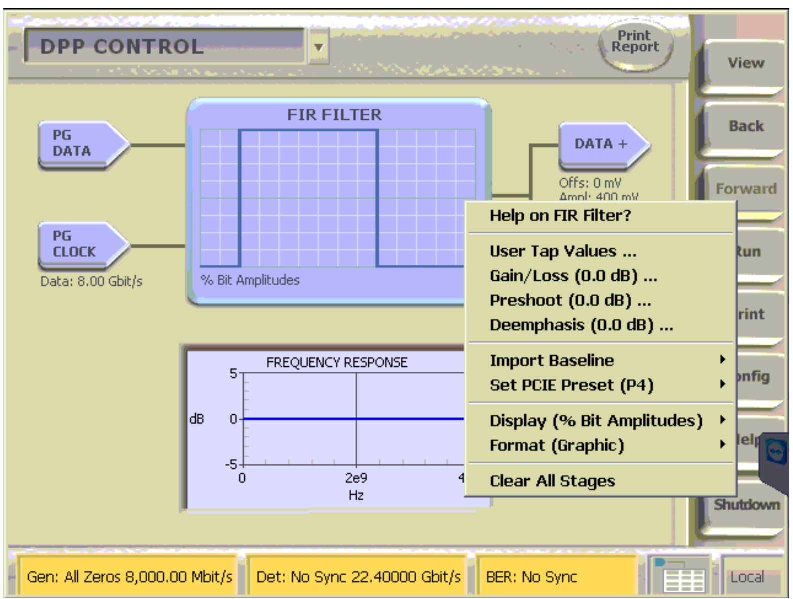


FIGURE 38. BERTSCOPE SETUP

9.1.1.2 Scope Setup & Measurement

1. Set the scope to Defaults.
2. Set scope Sampling mode to Real Time Only.
3. Set scope acquisition to average with 256 waveforms.
4. Set the trigger of A_Event type to timeout.
5. Set Chan1 and Chan2 display to ON; configure the scale and offset so the waveform covers 80% of the screen.
6. Enable Math1; set Math1 to Ch1-Ch2; set the auto scale.
7. Turn off Chan1 and Chan2.
8. Acquire Waveform. An example is shown in Figure 39.

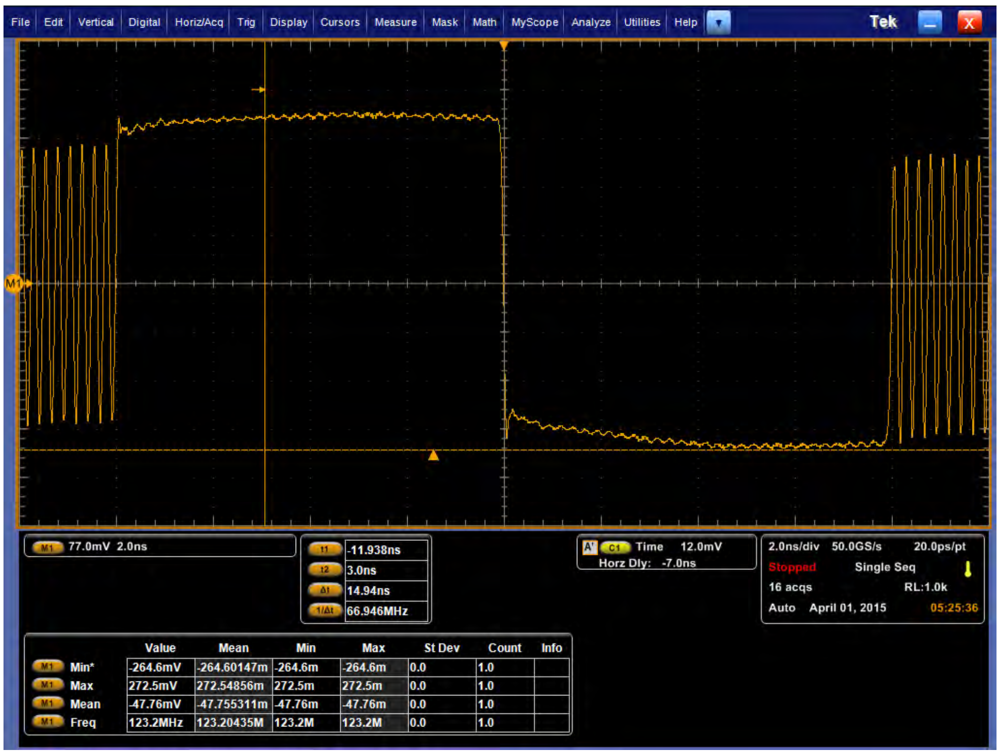


FIGURE 39. SCOPE SETUP AND MEASUREMENT

9.1.1.3 Deemphasis Measurement

Now, the actual de-emphasis and pre-shoot must be verified on scope.

1. Using cursors, measure peak-to-peak transition amplitude as shown Figure 40.

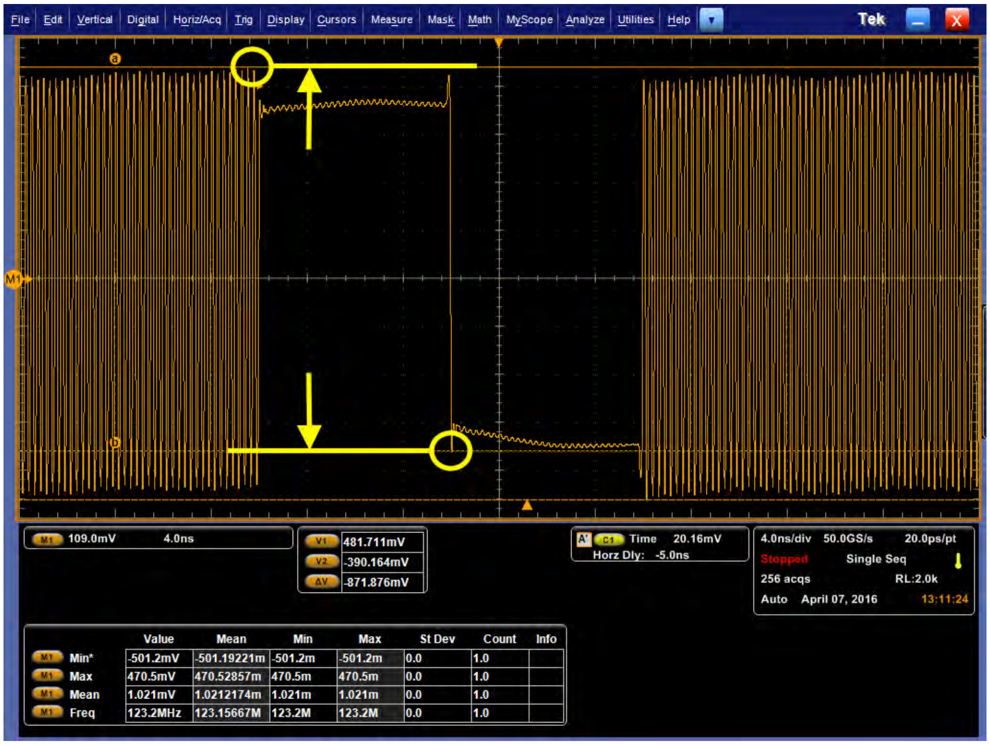


FIGURE 40. MEASURED TRANSITION AMPLITUDE (EXAMPLE 825MVPP)

2. Using cursors, measure peak-to-peak non-transition amplitude, as shown in Figure 41.

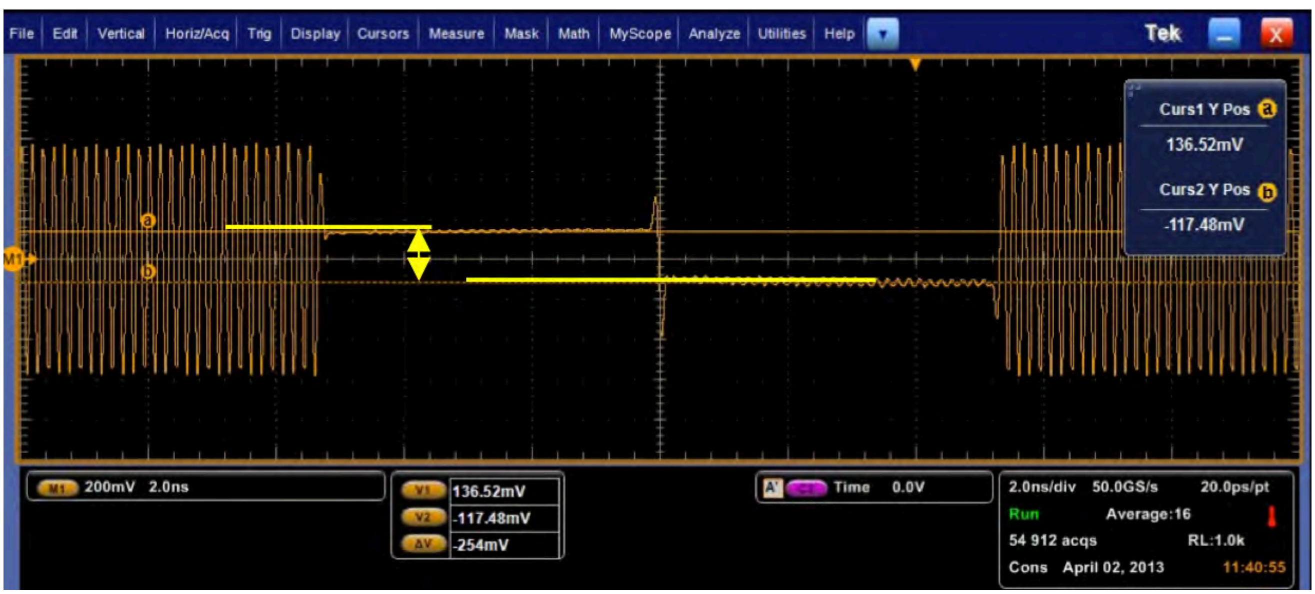


FIGURE 41. MEASURED NON-TRANSITION AMPLITUDE (EXAMPLE 254MV)

3. De-emphasis = 20log[Non-transition/Transition]

= 20log[254mV/824mV]

= 20log[0.31]

=-10.2dB

9.1.1.4 Preshoot Measurement

1. Using cursors, measure pre-shoot amplitude, as shown in Figure 42.

FIGURE 42. MEASURED PRESHOOT AMPLITUDE (EXAMPLE 622MV)

2. Measure pre-shoot amplitude.
3. Calculate the pre-shoot: 20log[Pre-shoot/Non-transition]

=20log[622 mV/254mV]
=20log[2.44]
=7.8dB

4. Increase the Preshoot and Deemphasis levels to record the measured Preshoot and Deemphasis dB for 3.5 and -6.0, measured respectively. See Figure 43 and Figure 44.
5. Record the value.

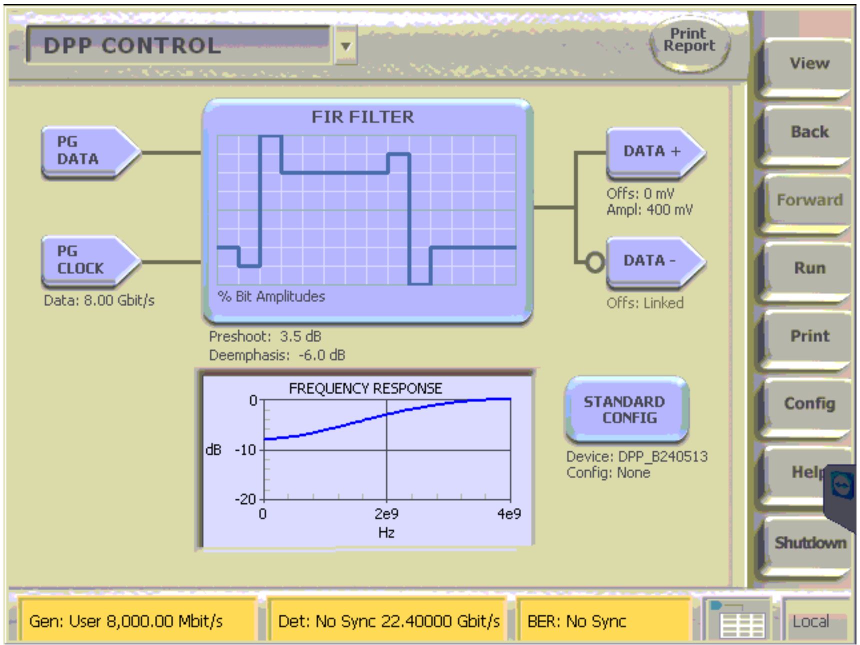


FIGURE 43. BERTSCOPE SETUP #2

FIGURE 44. SCOPE SETUP AND MEASUREMENT #2

9.1.2 Launch Amplitude

The Launch Amplitude is calibrated for target minimum peak-to-peak amplitude of 800mVpp after combiner.

9.1.2.1 BERTScope Setup

1. Using the same TP1 Calibration Setup.
2. Set DPP to 0.0 for Preshoot and Deemphasis.
3. Set DPP Amplitude to 300mV.
4. Set Pattern to Clk/256.

9.1.2.2 Scope Setup and Measurement:

1. Using the same Setup, Scale Chan1 and Chan2 respectively .
2. Turn off Chan1 and Chan2.
3. Turn On Math1, set to ch1-ch2.
4. Set the Acquisition mode to Average of 256
5. Set Measure Amplitude of Math1.
6. Acquire waveform.
7. Read the MEAN value of amplitude measurement.
8. Tune the DPP Output until Amplitude measured in scope is 800mV.

9.1.3 Amplitude Equalization

Perform the equalization of low frequency and high frequency amplitude at TP1. This is done by adding small amount of Deemphasis of DPP, so that low frequency and high frequency have the same amount of amplitude after combiner.

1. Using the same setup of calibration for TP1, and same BERTScope and TekScope setting.
2. Tune the DPP Pre Cursor and Post Cursor so Deemphasis is 0.0dB.
3. Tune the DPP Post Cursor until the low frequency and high frequency component of amplitude is same level. See Figure 45.

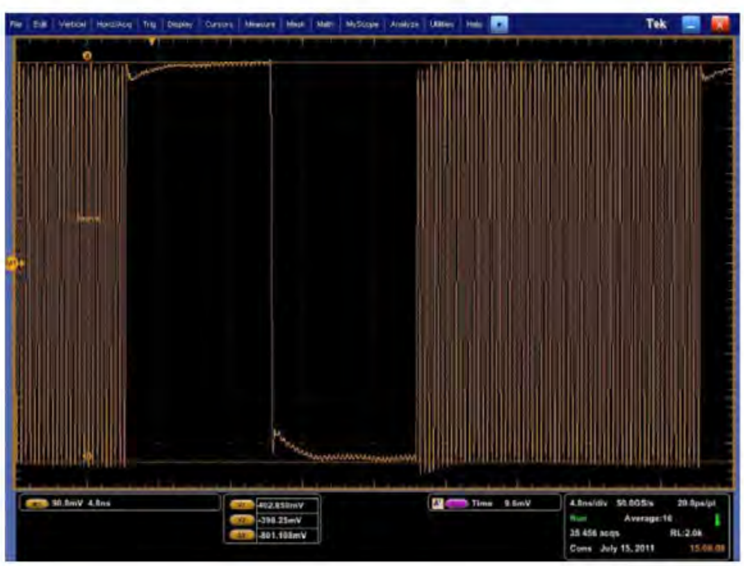


FIGURE 45. AMPLITUDE EQUALIZATION SETUP

4. Save the Post Cursor value.

9.1.4 RJ Calibration

1. Using a Clock pattern (1100), the RJ value of 0ps - 5ps will be calibrated. (Both limits are RMS values.) RJ is used to adjust the Eye Width (EW) in Stress Jitter Test.
2. RJ target is 2ps (RMS).
3. Tektronix DPOJET is used as the calibration tool.

9.1.4.1 BERTScope Setup

1. Set the Generator to 8Gpbs.
2. Set the Sub-rate clock mode is Stressed Clock.
3. Set the RJ Enable.
4. Set the SJ Enable, Set the SJ Amplitude to 0.0mV. See Figure 46.

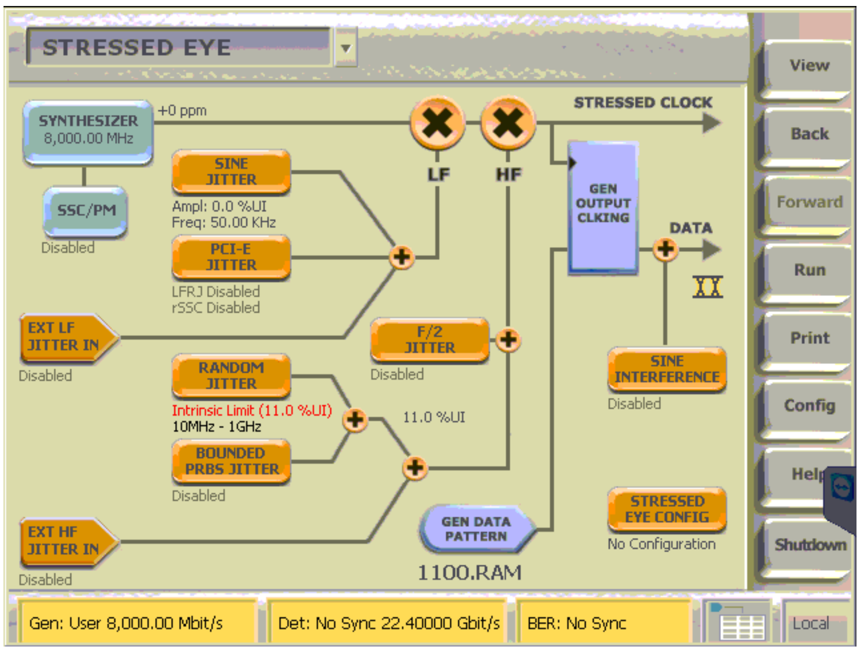


FIGURE 46. BERTSCOPE JITTER SETUP

5. Set the Pattern of generator to 1100.ram (1-1-0-0 pattern). See Figure 47.

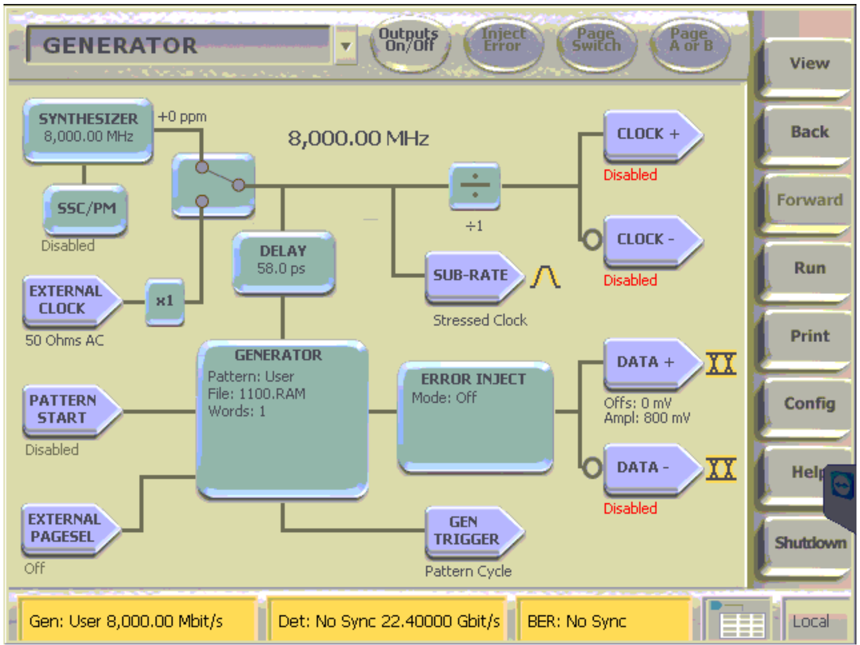


FIGURE 47. BERTSCOPE PATTERN SETUP

9.1.4.2 DPP Setup

1. Set the DPP PreShoot and DeEmphasis using P4 preset (0.0db for both).
2. Set the post cursor and pre cursor based on equalized amplitude value recorded earlier.
3. Set DPP output that reflect 800mV amplitude that recorded earlier.

9.1.4.3 Scope Setup

1. Set the DPOJET Configure - > Clock Recovery to Constant Clock Mean.

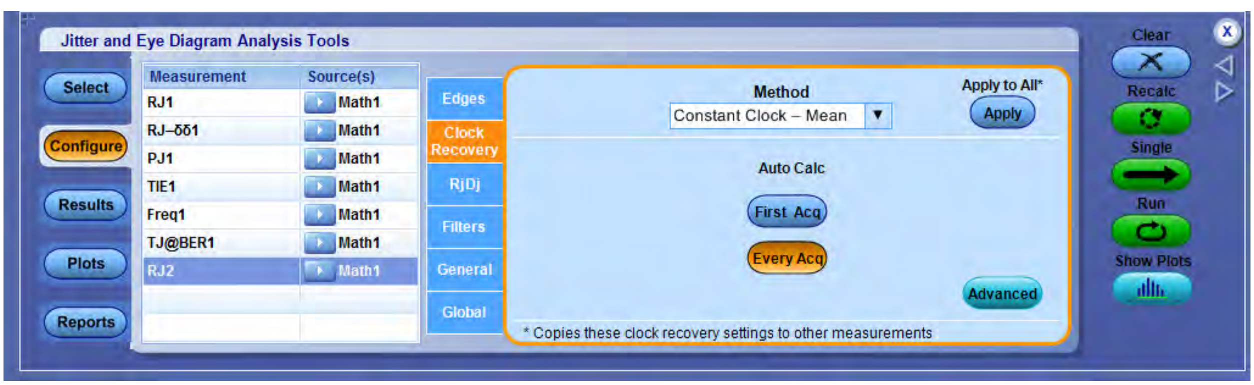


FIGURE 48. DPOJET CONFIGURE SETUP

2. Under RJDJ settings for clock signal.

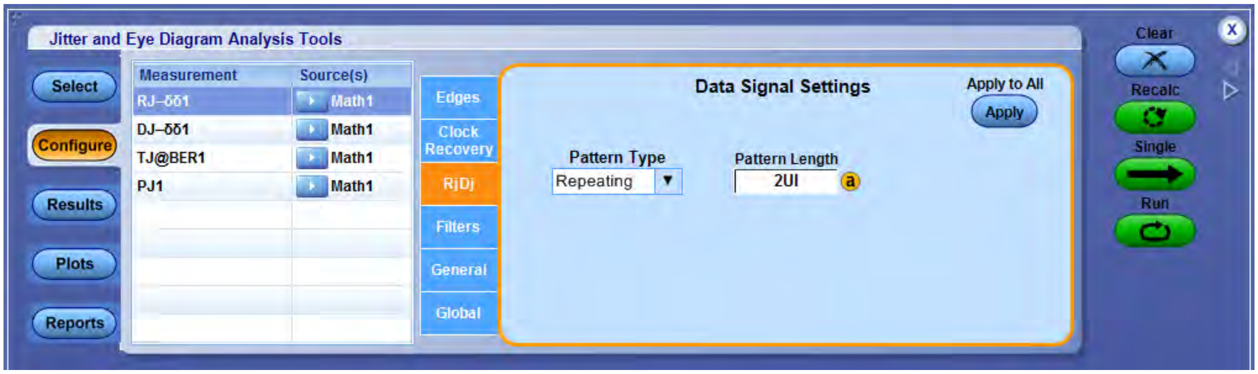


FIGURE 49. RJDJ SETUP

3. On the Advance Panel, set the Nominal Data Rate to 8Gpbs.

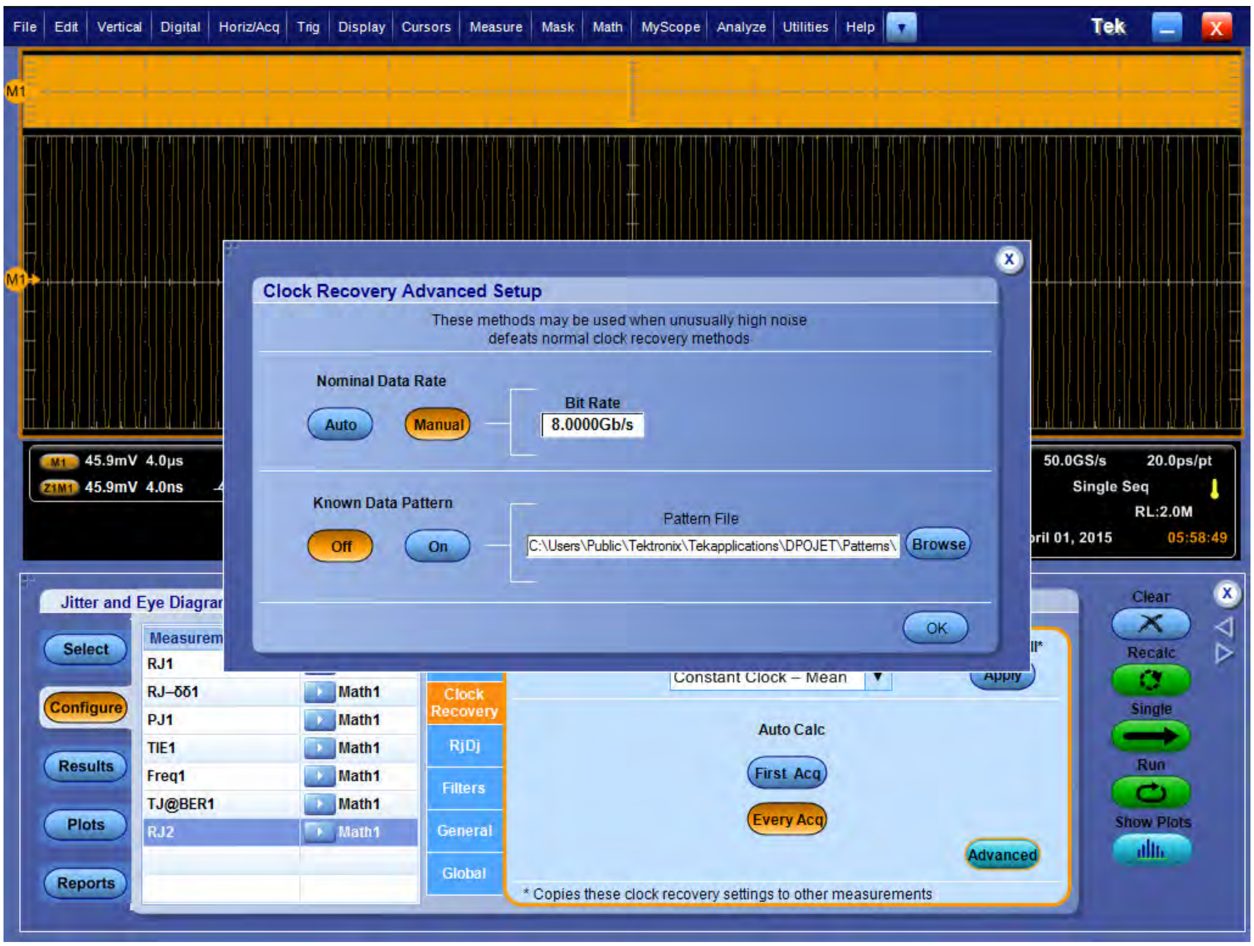


FIGURE 50. SCOPE ADVANCED SETUP

4. Set the Horizontal mode to Manual, set record length to 2M.

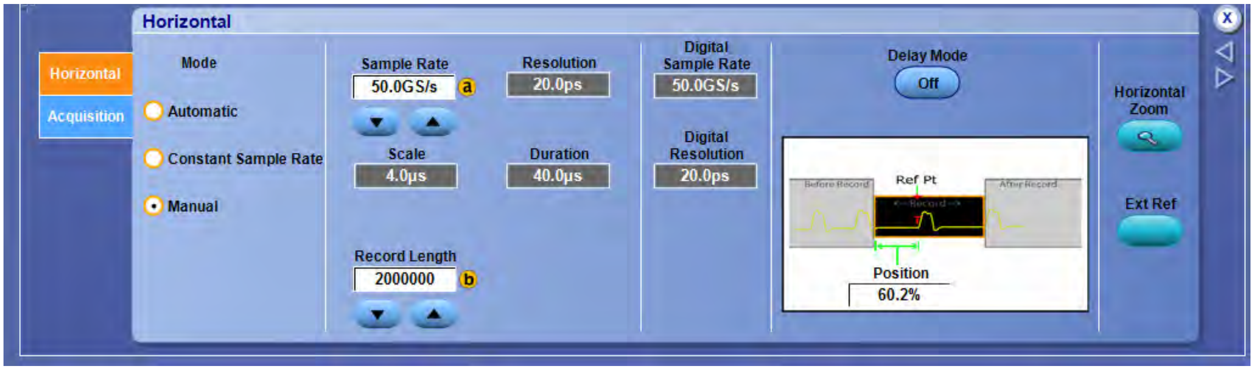
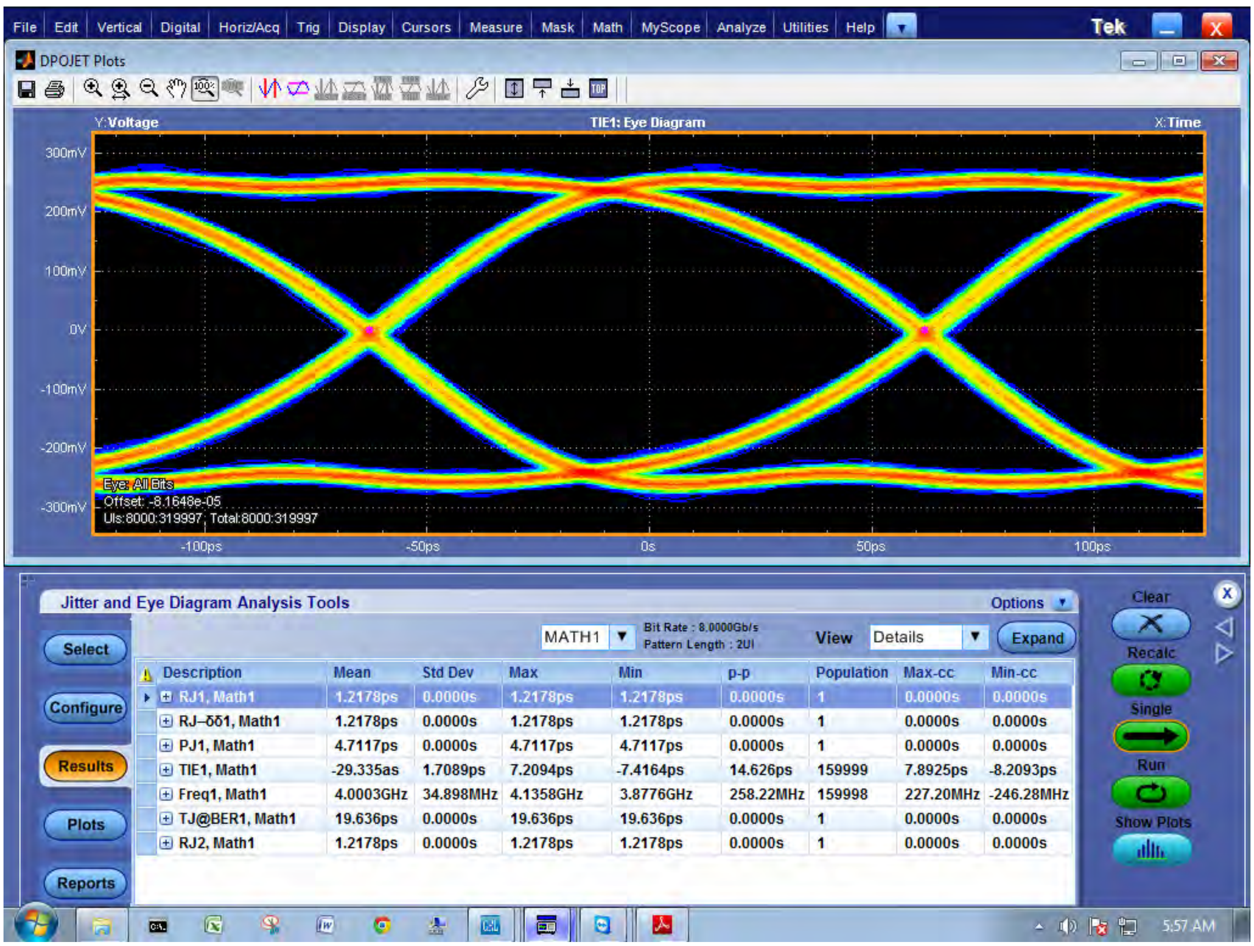


FIGURE 51. SCOPE RECORD LENGTH SETUP

5. Clear the result. Run Single.



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
RJ1, Math1	1.2178ps	0.0000s	1.2178ps	1.2178ps	0.0000s	1	0.0000s	0.0000s
RJ–δδ1, Math1	1.2178ps	0.0000s	1.2178ps	1.2178ps	0.0000s	1	0.0000s	0.0000s
PJ1, Math1	4.7117ps	0.0000s	4.7117ps	4.7117ps	0.0000s	1	0.0000s	0.0000s
TIE1, Math1	-29.335as	1.7089ps	7.2094ps	-7.4164ps	14.626ps	159999	7.8925ps	-8.2093ps
Freq1, Math1	4.0003GHz	34.898MHz	4.1358GHz	3.8776GHz	258.22MHz	159998	227.20MHz	-246.28MHz
TJ@BER1, Math1	19.636ps	0.0000s	19.636ps	19.636ps	0.0000s	1	0.0000s	0.0000s
RJ2, Math1	1.2178ps	0.0000s	1.2178ps	1.2178ps	0.0000s	1	0.0000s	0.0000s

FIGURE 52. SCOPE WAVEFORM CAPTURE

6. Read the measured RJ1.

7. Tune the BertScope RJ value.

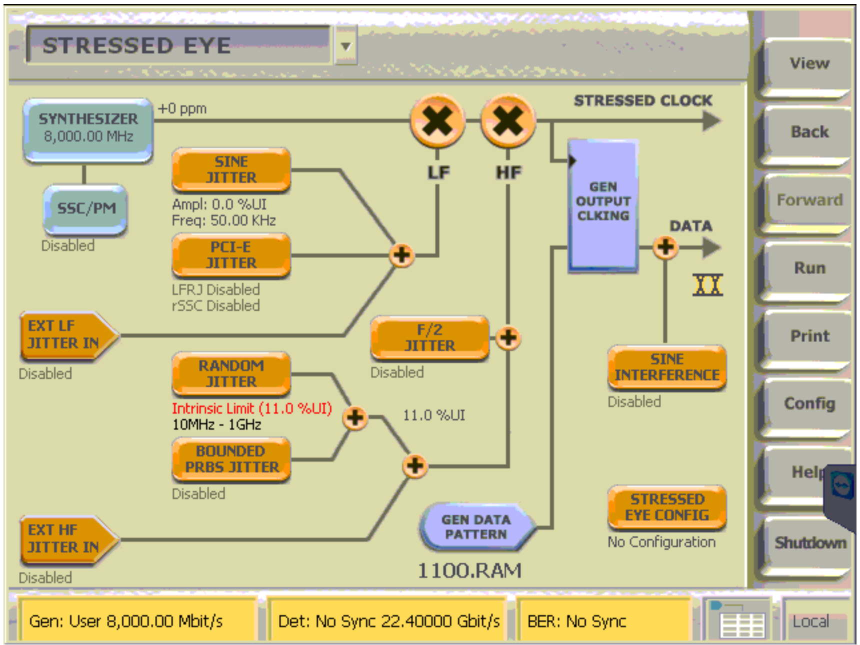


FIGURE 53. BERTSCOPE RJ CAPTURE

8. The target measured value for RJ: 2ps RMS and 3ps RMS.

9.1.5 SJ Calibration

There are four SJ (Sweep Jitter) frequencies required: 30KHz, 1MHz, 10MHz and 100MHz. SJ needs to be calibrated (with 1100 pattern) for all cases in the proper way.

TABLE 4. STRESSED JITTER TESTS

Frequency		
30KHz		
1MHz		
10MHz		
100MHz	0.1	UI PP

Stressed Voltage Test:

$T_{RX\text{-}SV\text{-}SJ\text{-}8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.

Stressed Jitter Test:

$T_{RX\text{-}ST\text{-}SJ\text{-}8G}$	Sinusoidal Jitter	0.1 – 1.0	UI PP	See Figure 4-74 Measured at TP1. See Note 3.

The Stressed Jitter test requires the test to pass each and every frequency, with its respective SJ amplitude at 30KHz, 1MHz, 10MHz and 100MHz.

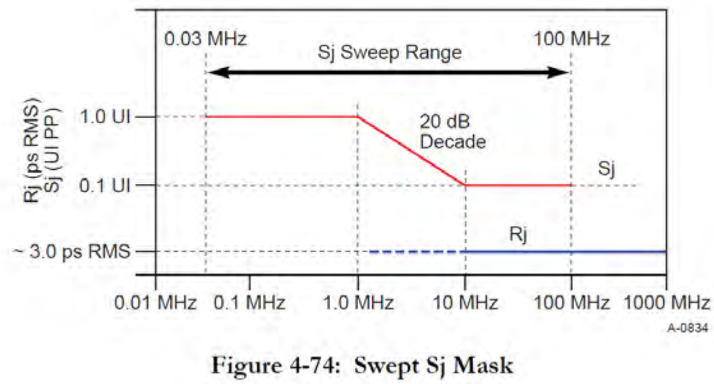


FIGURE 54. SWEEP JITTER RANGE AND MASK

Using this same setup at each frequency, make the measurement.

9.1.5.1 Calibrate Sweep Jitter at 30KHz.

1. On BERTScope, Enable ***Phase Modulator*** and Set *PM Frequency* to 30KHz and *PM Devn: 1UI*.

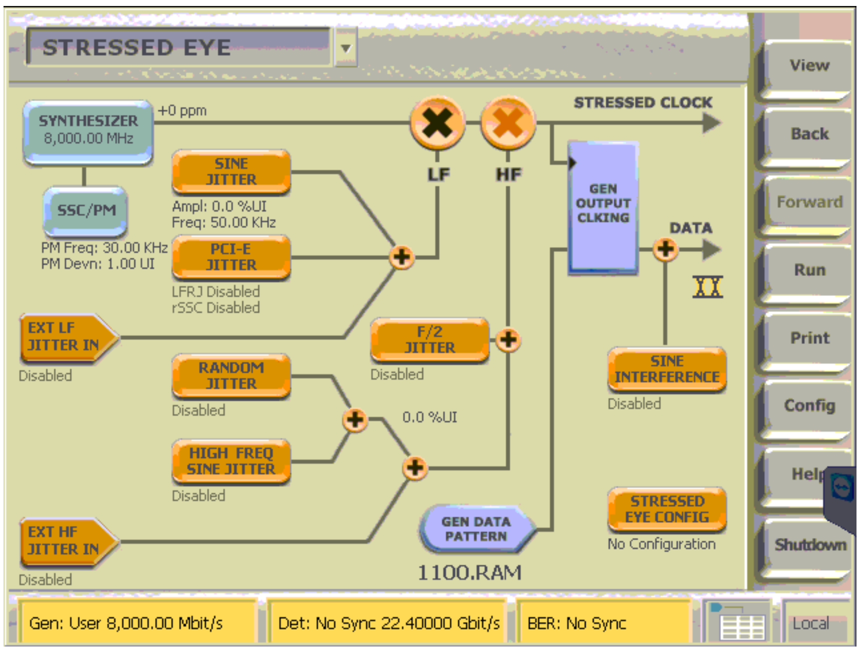


FIGURE 55. SWEEP JITTER BERTSCOPE SETUP AT 30KHZ

2. On the BERTScope, using DPOJET, measure PJ1. Note, for this measurement the DPOJET Clock Recovery Method should be set to Constant Clock – Mean so as to not filter the low frequency jitter modulation that is to be verified.
3. Read the PJ1 measurement. It is in units of seconds. Convert to UI.

9.1.5.2 Calibrate Sweep Jitter at 1MHz, 10MHz, 100MHz

1. Set Sine Jitter initially to 10% UI.

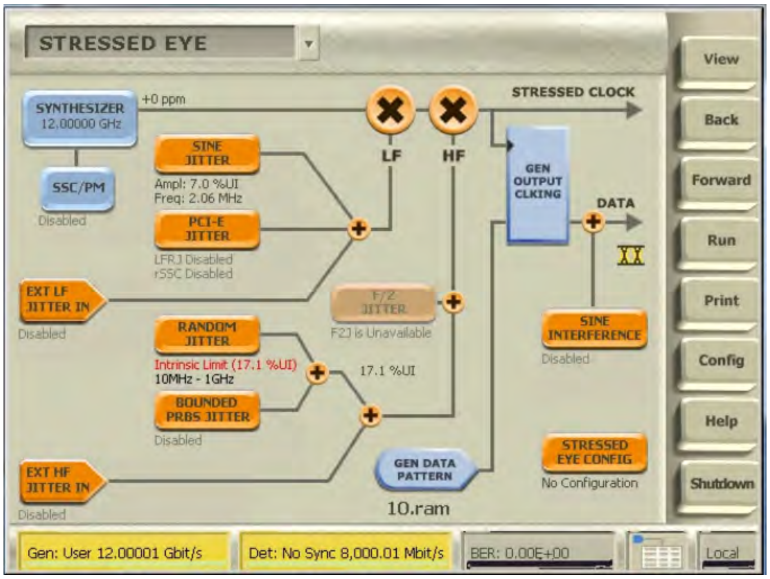


FIGURE 56. SWEEP JITTER BERTSCOPE SETUP AT 1MHZ-100MHZ

1. Measure SJ using DPOJET.

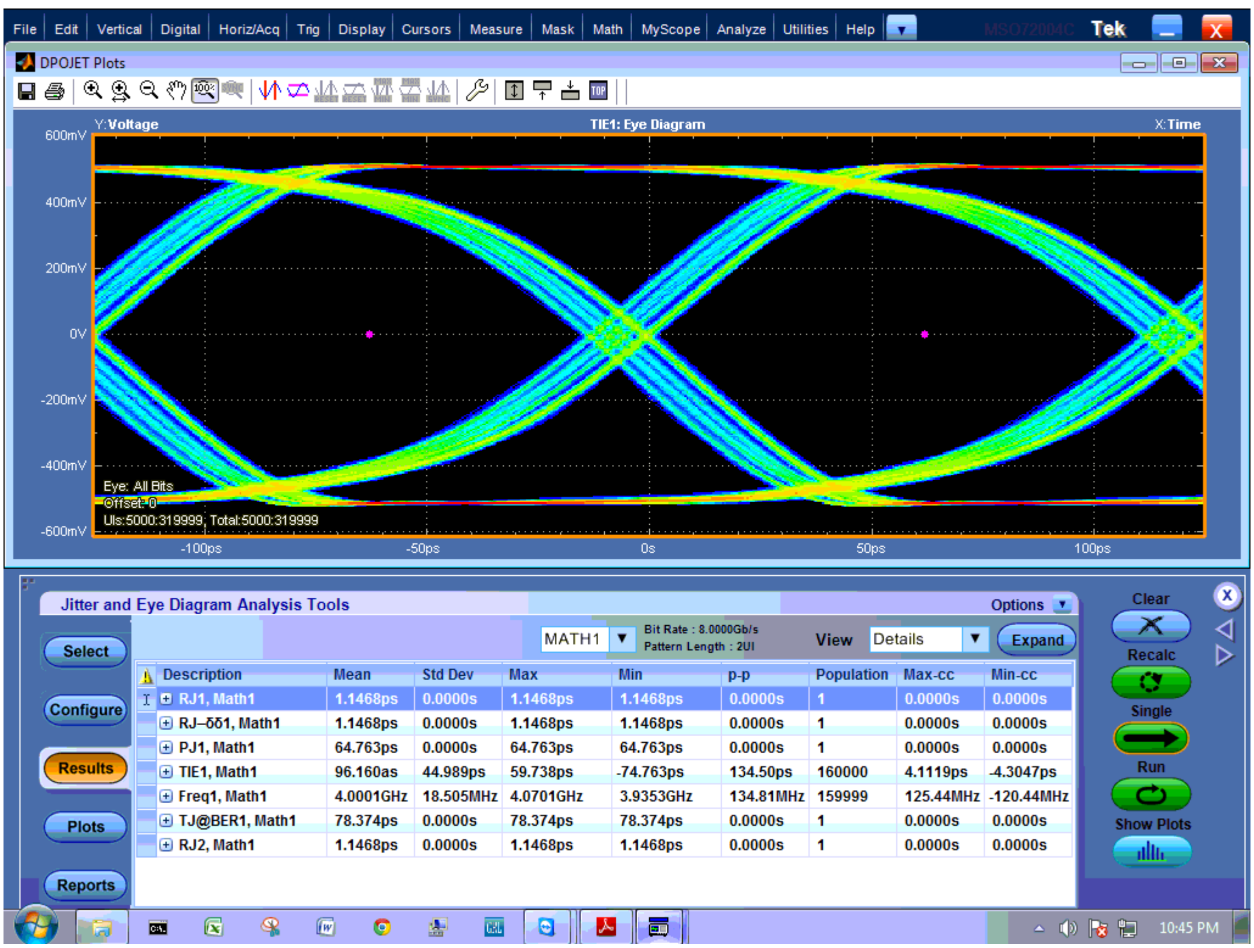


Figure 57. Sweep Jitter DPOJET Measurement at 1MHz-100MHz

2. Read the PJ1 value.
3. Again, note value of SJ on BERTScope needed to generate 10% SJ at reference point.
4. Calibration for 1MHz, 10MHz and 100MHz will need to set the SJ Frequency and SJ Amplitude instead of PM.

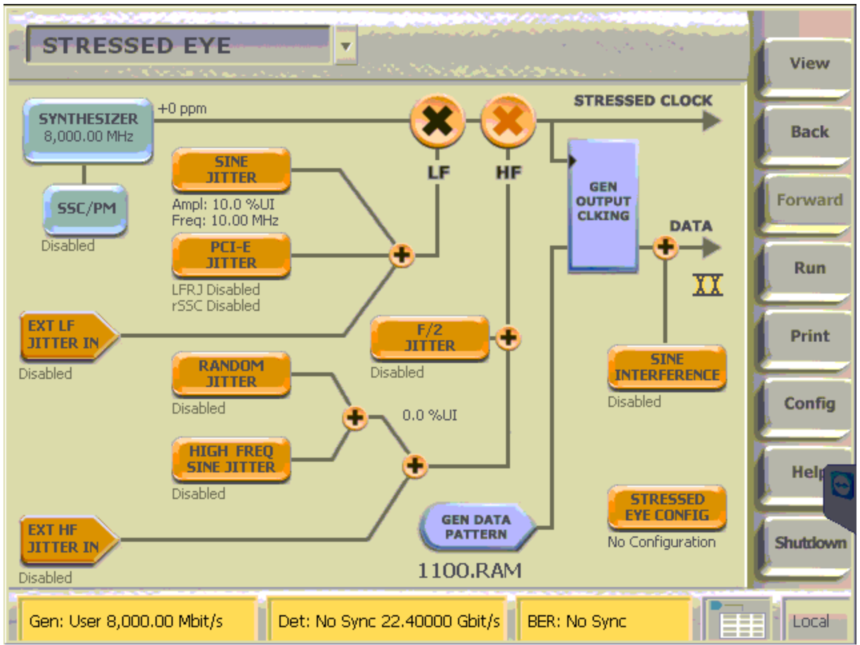


Figure 58. Calibration at 1MHz-100MHz

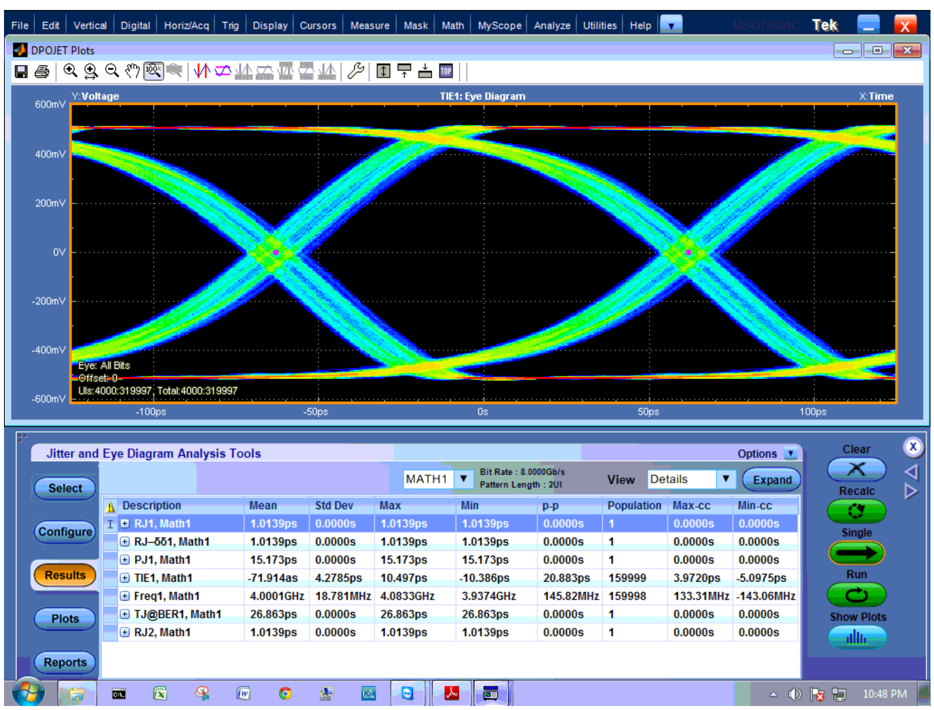


Figure 59. Sweep Jitter DPOJET Measurement at 1MHz-100MHz

9.2 Channel Calibration Tests (TP2)

9.2.1 Channel Calibration Insertion Loss

PCIe Gen3 defines 3 types of calibration channel.

1. None
2. Short
3. Long

Defined by Figure 60, each channel insertion loss must meet the mask depending on its channel type. Variable and programmable ISI injector is needed to simulate the trace length to achieve the target loss for each channel.

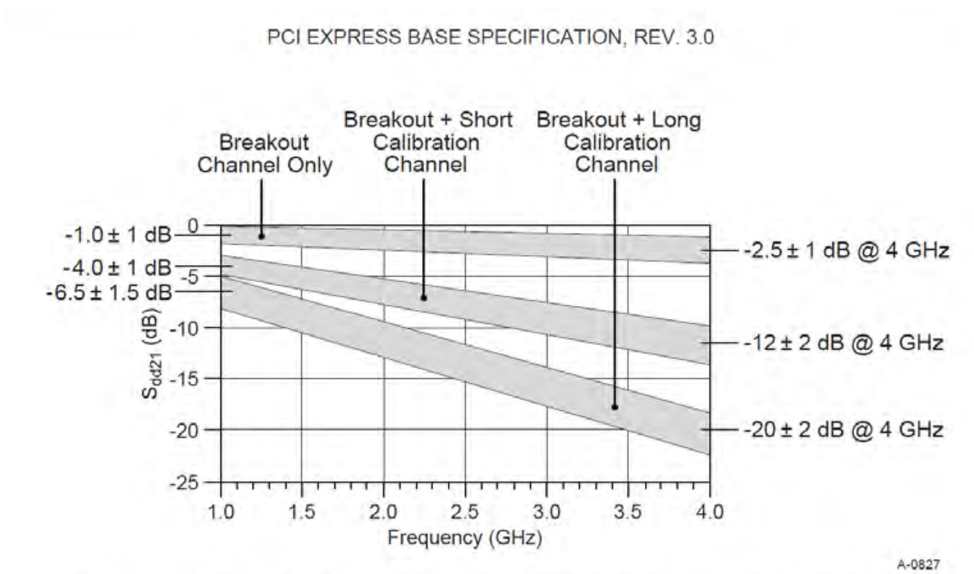


FIGURE 60. CHANNEL INSERTION LOSS MASK BY CHANNEL TYPE

Insertion loss is measured by differentiating step response, and doing the FFT of the resulting impulse response. The Seasim application provides the method to calculation the insertion loss given the step response.

9.2.1.1 BERTScope Setup

1. Set BERTScope Set Pattern to clk/256.
2. Set DPP Set Deemphasis and Preshoot to P4 with post cursor and pre cursor for equalization of amplitude recorded earlier.
3. Set DPP output that reflects the 800mV amplitude that was recorded earlier.
4. Disable Rj.
5. Disable Sj.

9.2.1.2 ISI Setup

1. Open the Artek ISI application.

2. Set the ISI % to 0.0.

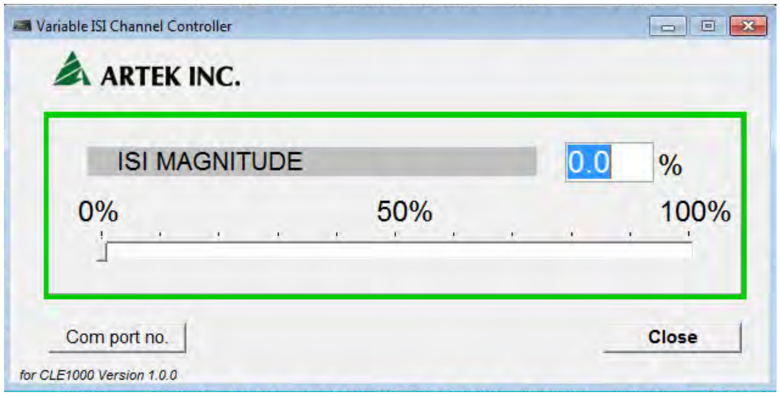


FIGURE 61. ISI SETUP

9.2.1.3 Scope Setup

1. Turn On Ch1 and Ch2, scale ch1 and ch2 correctly.
2. Turn Off ch1 and ch2
3. Turn ON Math1, set ch1-ch2. Scale correctly.
4. Setup Trigger A Event to Edge, source to chan1,
5. Setup Trigger A-B Event with Acquisition Delay to 4ns.

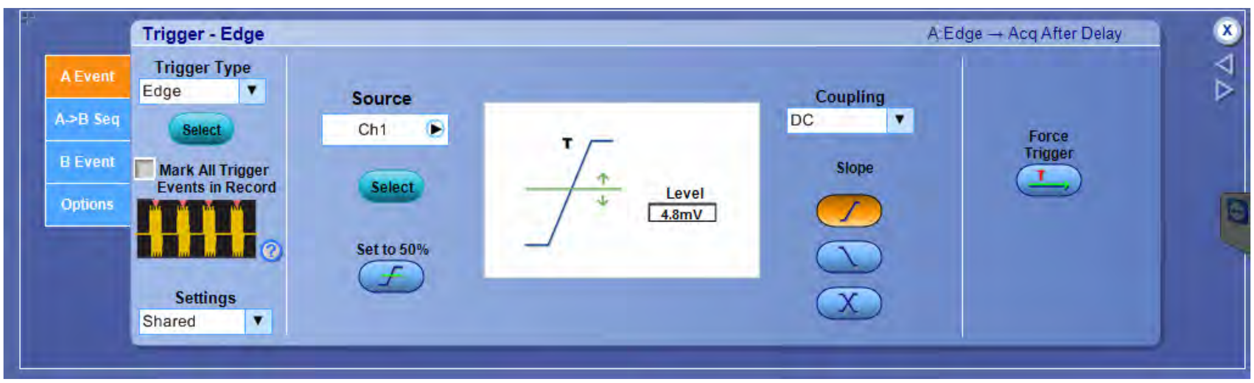


FIGURE 62 SCOPE SETUP #1

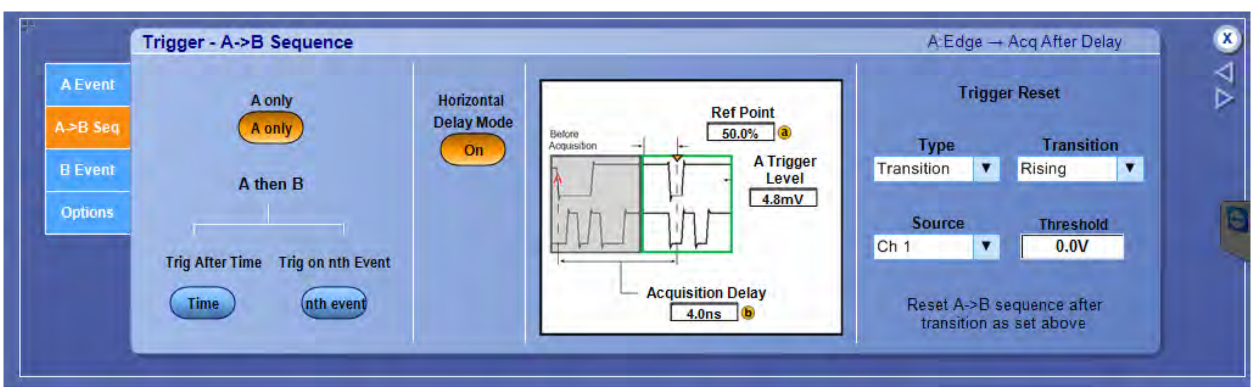


FIGURE 63 SCOPE SETUP #2

6. Setup Acquisition Mode to Average of 2048 Waveforms.

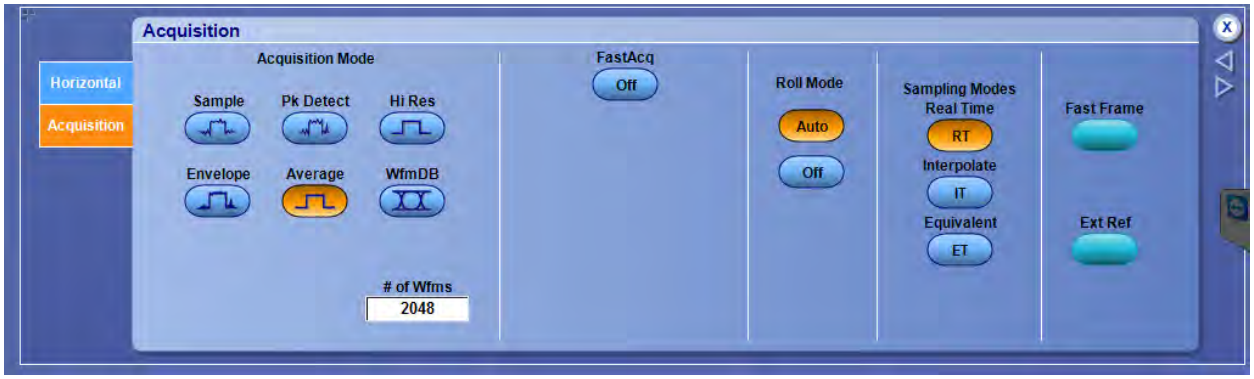


FIGURE 64 SCOPE ACQUISITION MODE SETUP

7. Run Single and capture measurement.

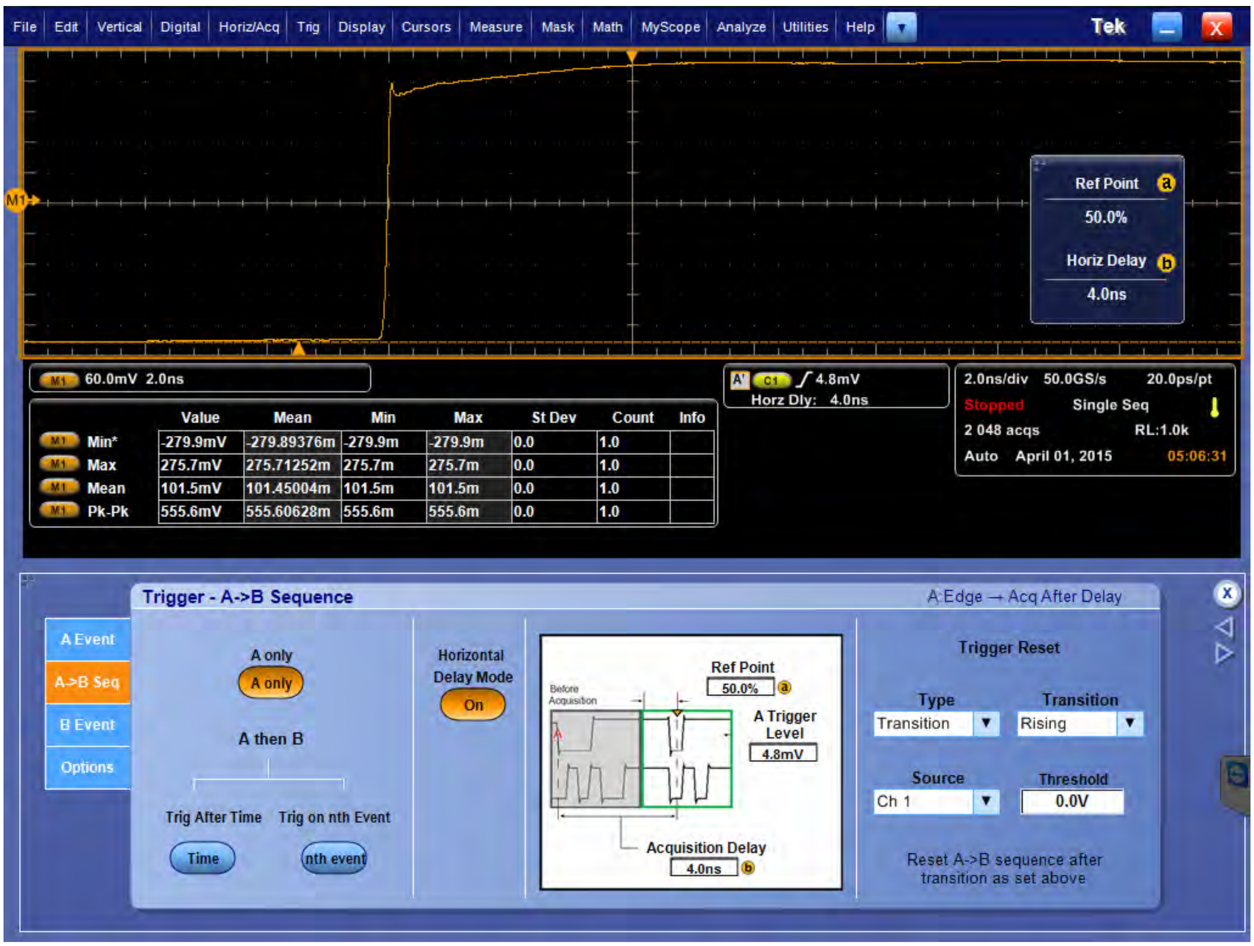


FIGURE 65 CAPTURE MEASUREMENT

8. Save the Waveform to .DAT format.
9. Modify the .dat format to Seasim compatible waveform with name ending _vict.rfstep1.
10. The _vict.rfstep1 format is consist of **time**[SPACE]**Voltage_level**[New Line].
11. Copy the _vict.rfstep1 step response to \step_response folder.

12. Launch Seasim_GUI.pyw.

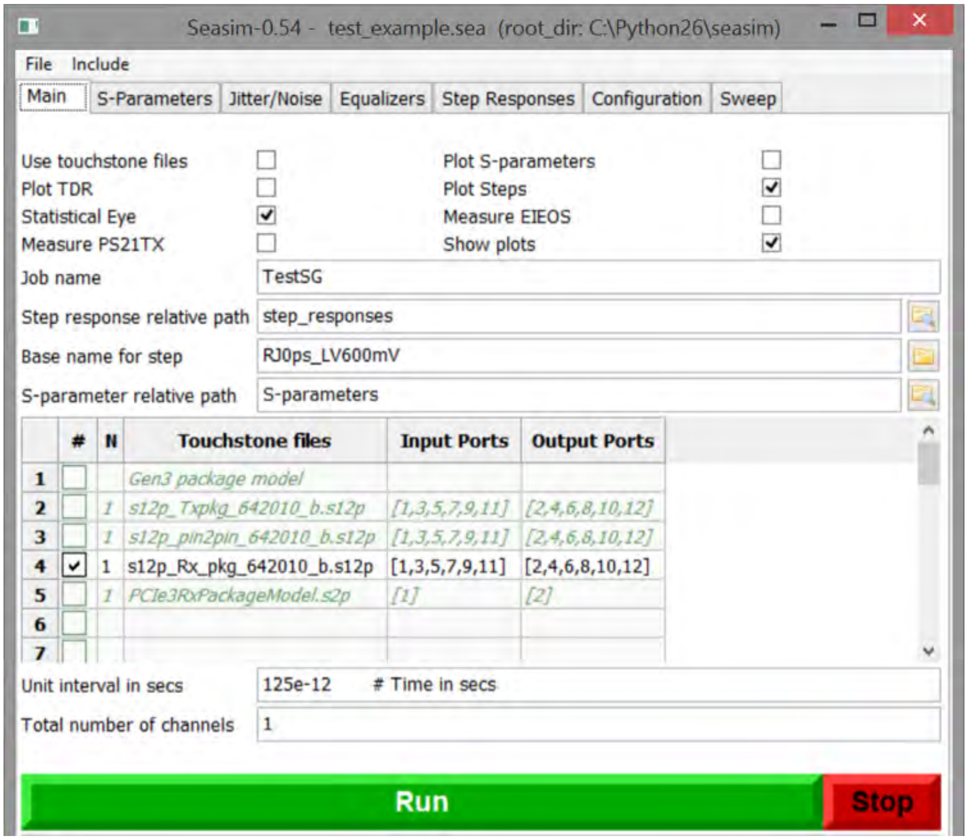


FIGURE 66 SAVE THE WAVEFORM

13. Change the file name Base name Step to the file name saved and modified.
14. Click Run.

15. Seasim will output graph indicating the insertion loss.

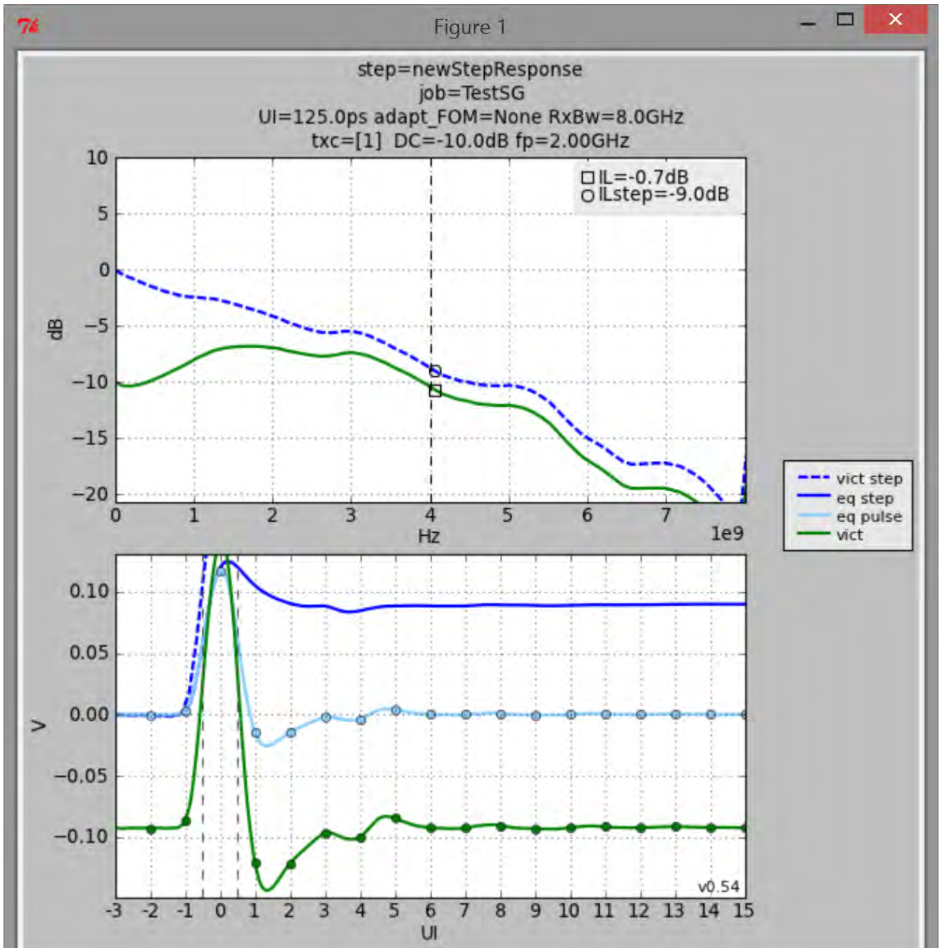


FIGURE 67 SEASIM INSERTION LOSS OUTPUT GRAPH

16. Insertion loss at 4GHz is -9dB for sample above.
17. Increase the ISI % then re capture the waveform, save, modify and run Seasim.
18. Ensure the insertion loss is between the PCIe Gen3 specs for respective channel type.

9.2.1.4 Example Results

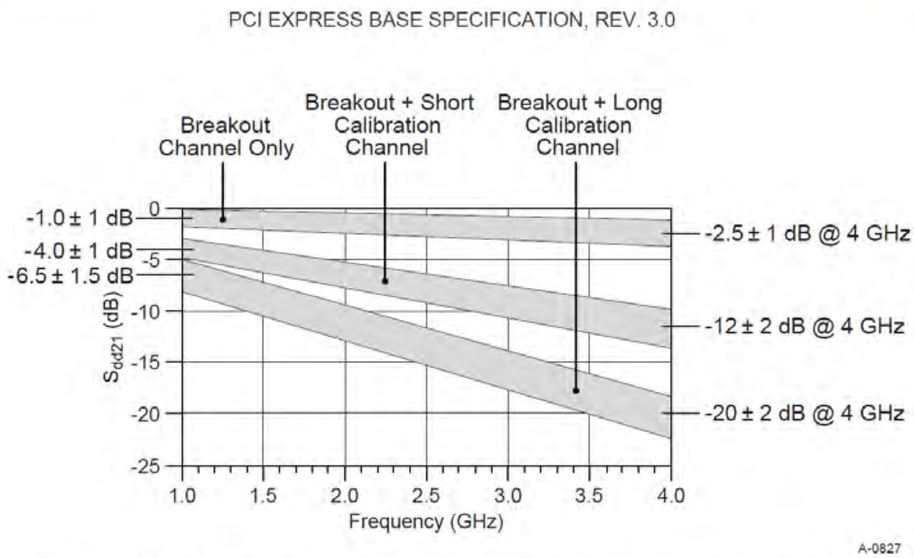


FIGURE 68 SPECIFICATION MASK

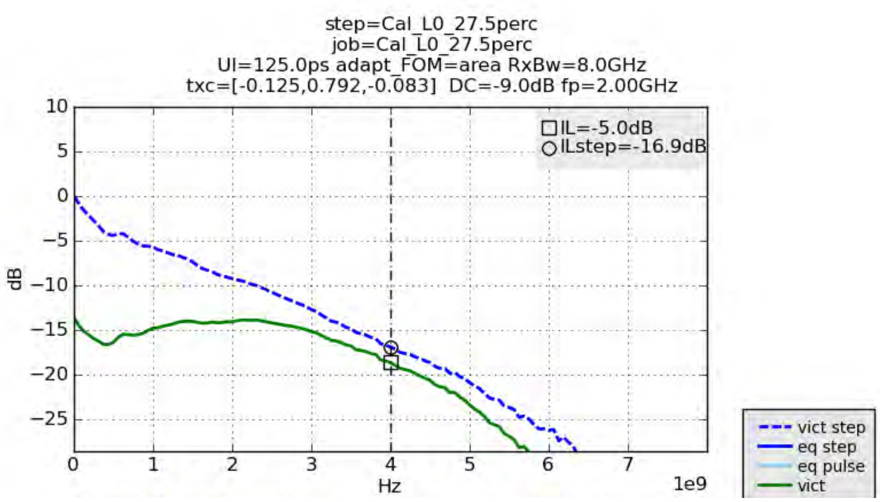


FIGURE 69 INSERTION LOSS AT 27.5% ISI (-16.9DB)

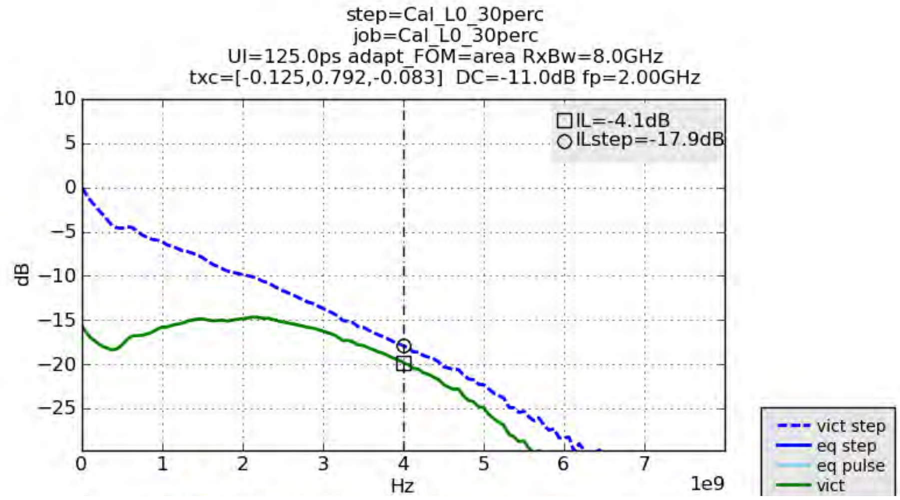


FIGURE 70 INSERTION LOSS AT 30.% ISI (-17.9DB)

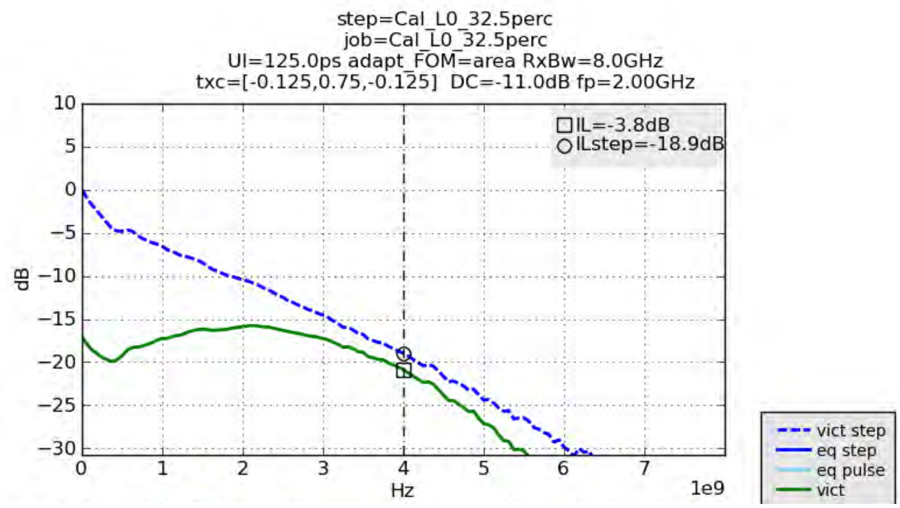


FIGURE 71 INSERTION LOSS AT 32.5% ISI (-18.9DB) WITHIN TARGET

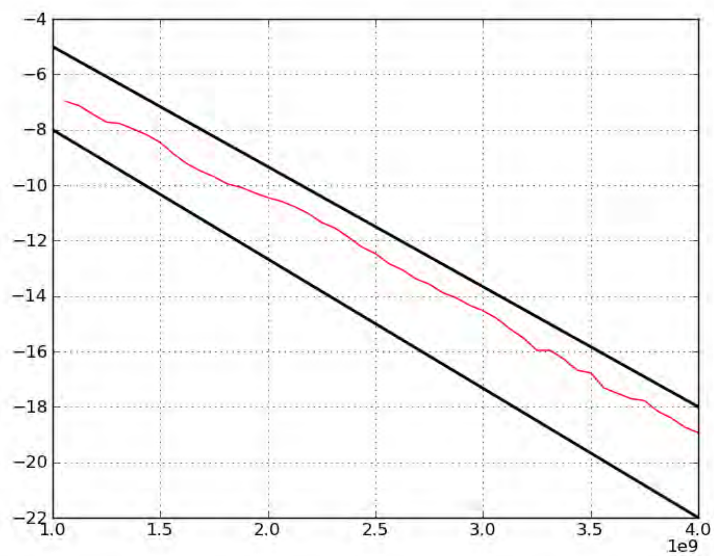


FIGURE 72 INSERTION LOSS CALIBRATION FOR LONG CHANNEL – IL FALLS BETWEEN REQUIRED MASK

9.2.2 Channel Calibration Differential Mode Sinusoidal Interference

9.2.2.1 BERTScope Setup

1. Set ALL ZERO Pattern.

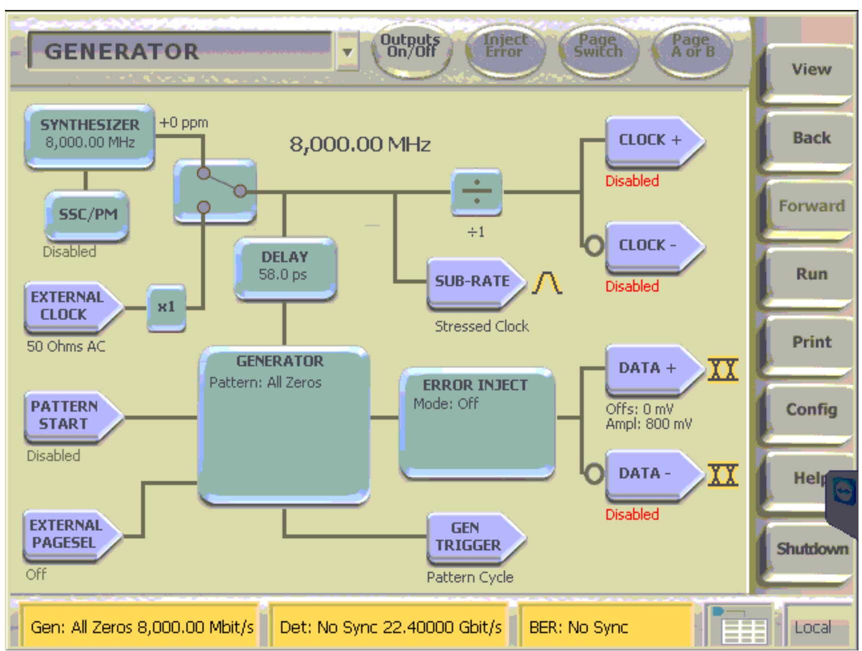


FIGURE 73 BERTSCOPE SETUP FOR ALL ZERO PATTERN

2. Set all Jitter to 0mV amplitude.
3. Enable the SINE INTERFERENCE.
4. Set the Frequency to 2.1GHz.
5. Set to External.

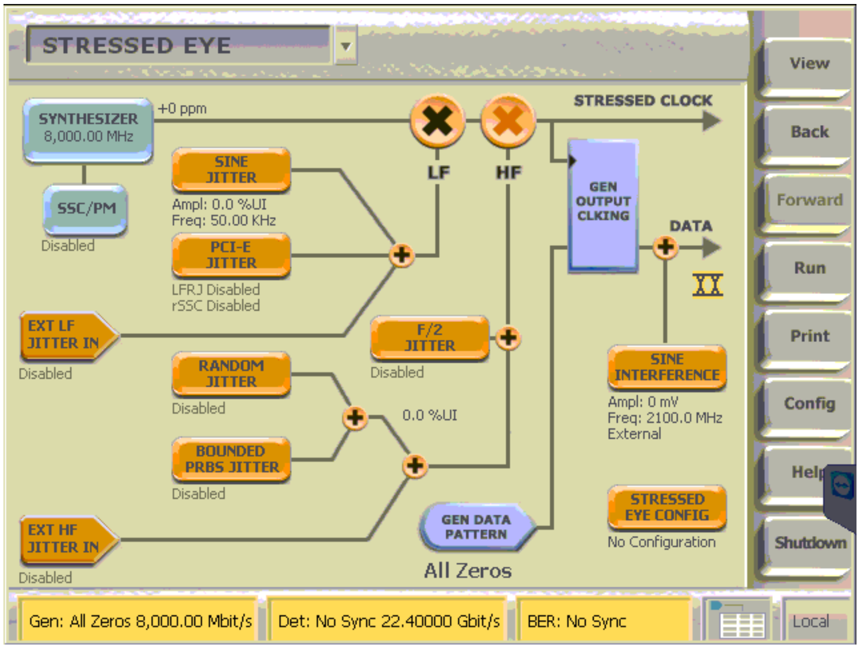


FIGURE 74 BERTSCOPE SETUP #2

6. Set the Sine Interference Amplitude to 100mV.

9.2.2.2 ISI Setup

1. Set the Artek ISI % to calibrated channel type.

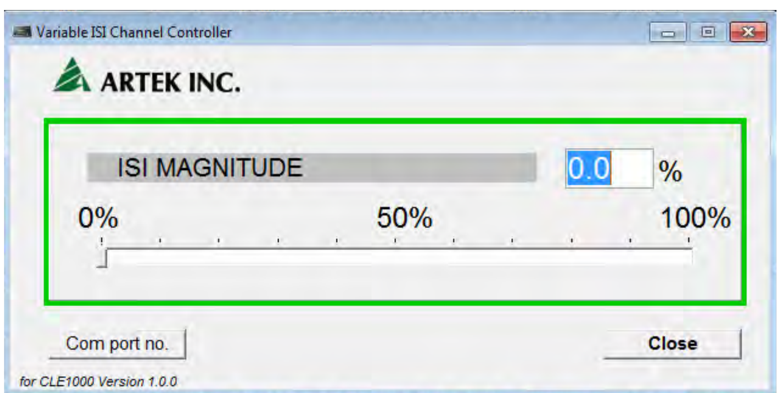


FIGURE 75 ARTEK ISI SETUP

9.2.2.3 Scope Setup

1. Set Acquisition Average to 256.
2. Scale Ch1 and Ch2 accordingly.
3. Turn on MATH1, ch1-ch2, scale accordingly.
4. Measure Peak to Peak of Math1.
5. Run Single.
6. Obtain the MEAN value of math1 peak to peak.
7. Tune the Sine Interference Amplitude so measured value is 16mV.

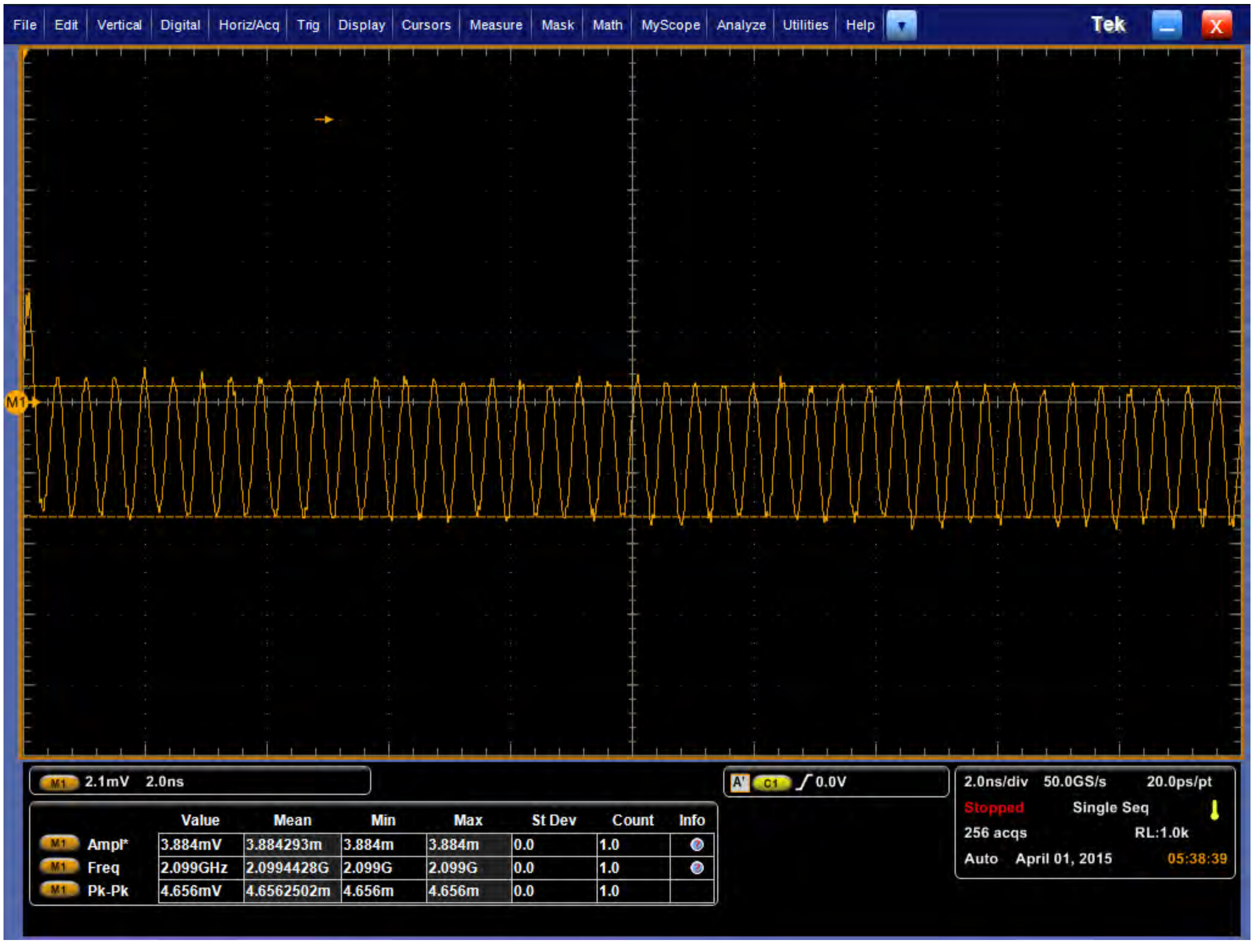


FIGURE 76 SCOPE MEASUREMENT

9.2.3 Channel Calibration AC Common Mode Sinusoidal Interference

9.2.3.1 BERTScope Setup

1. Remain ALL ZERO Pattern.
2. Set the SINE Interference amplitude to 0mV.

9.2.3.2 Setup AFG

1. Enable the AFG output 1.
2. Set the Output Mode to SINE wave.
3. Set the SINE Wave frequency to 120MHz.
4. Set the Output1 Amplitude to 1V.

9.2.3.3 Scope Setup

1. Scale Ch1 and Ch2.
2. Set MATH1 to ch1+ch2.Scale MATH1.
3. Turn OFF Ch1 and CH2.
4. Set Acquisition to Average 256.

FIGURE 77 SCOPE MEASUREMENT

5. Tune the AFG Amplitude.
6. Target CM:

    150mV for Long Channel

    250mV for Short and None Channel

9.3 Calibration at TP2P

Two distinct tests are utilized to test a receiver: one for its minimum eye height (voltage), and another for its minimum eye width (jitter). The procedures for calibrating the stressed eye are similar, although the number and magnitude of signal impairment sources varies between the two tests.

9.3.1 TP2P Stressed Voltage Calibration

The configuration for calibrating a stressed voltage eye for Rx testing is shown below where the calibration procedure is performed for all three calibration/breakout channel combinations. Rj and Sj are added as defined in below and common mode and differential mode noise sources are added simultaneously.

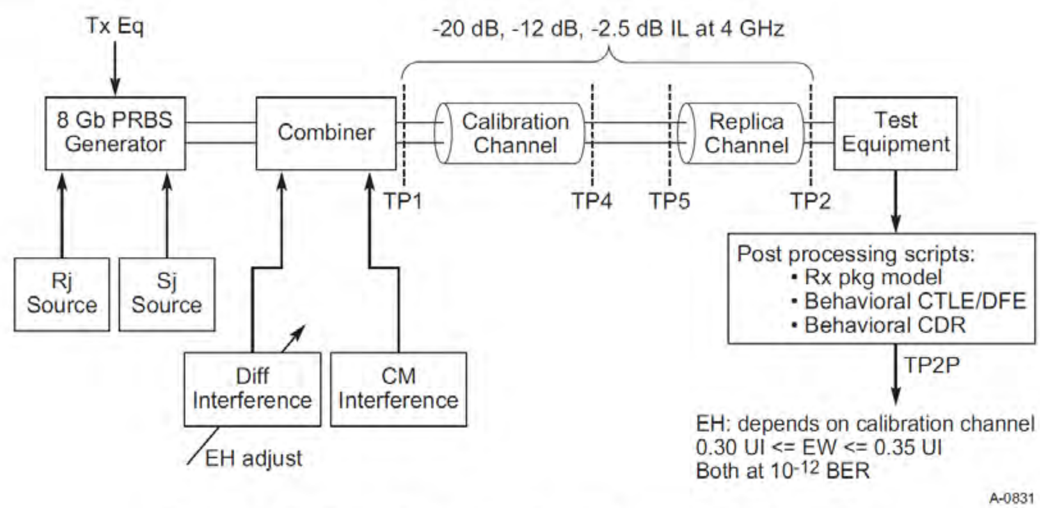


Figure 4-71: Setup for Calibrating the Stressed Voltage Eye

FIGURE 78 SETUP FOR CALCULATING THE STRESSED VOLTAGE EYE

Table 4-22: Stressed Voltage Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX\text{-}LAUNCH\text{-}8G}$	Generator launch voltage	800	mVPP	Measured at TP1 Figure 4-65. $V_{RX\text{-}LAUNCH\text{-}8G}$ may be adjusted if necessary to yield the proper EH as long as the outside eye voltage at TP2 does not exceed 1300 mVPP.
$T_{RX\text{-}UI\text{-}8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX\text{-}SV\text{-}8G}$	Eye height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mVPP	Eye height @ BER=10^{-12}. Notes 1,2.
$T_{RX\text{-}SV\text{-}8G}$	Eye width at TP2P	0.3 to 0.35	UI	Eye width at BER=10^{-12}. Note 2
$V_{RX\text{-}SV\text{-}DIFF\text{-}8G}$	Differential mode interference	14 or greater	mVPP	Adjusted to set EH. Frequency = 2.10 GHz. Note 3.
$V_{RX\text{-}SV\text{-}CM\text{-}8G}$	Rx AC Common mode voltage at TP2P	150 (EH < 100 mVPP) 250 (EH ≥ 100 mVPP)	mVPP	Defined for a single tone at 120 MHz. Note 3.
$T_{RX\text{-}SV\text{-}SJ\text{-}8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.
$T_{RX\text{-}SV\text{-}\text{-}RJ\text{-}8G}$	Random Jitter	2.0	ps RMS	Rj spectrally flat before filtering. Notes 4,5.
$V_{RX\text{-}MAX\text{-}SE\text{-}SW}$	Max single-ended swing	±300	mVP	Note 6.

FIGURE 79 STRESSED VOLTAGE EYE PARAMETERS

Eye width and eye height are defined after applying post processing and are defined at TP2P. The long calibration channel utilizes both CTLE and DFE, while the medium and short channels calibration channels use CTLE only.

EH is set by adjusting the amount of differential noise until the value defined by VRX-SV-8G is obtained. If it is not possible to maintain a sufficient eye width by adjusting only the differential noise, it is acceptable to inject less differential noise and adjust the generator launch voltage.

Seasim is used to post process the receiver eye at TP2P.

In this context, Rj, Sj, DM-SI source are input to Seasim. While CM SI are combined with clk/256 pattern source from BERT and captured in Scope.

9.3.1.1 BERTScope Setup

1. Set BERTScope Pattern to clk/256
2. Turn Off Rj, Sj, DM-Si at BERTScope.
3. Set DPP Ouput to 800mV Amplitude calibrated earlier.
4. Set DPP DeEmphasis and Preshoot. Use "Preset 4 for Short and None channel. Use Preset 7 for Long channel.

9.3.1.2 AFG Setup

1. Turn Off AFG

9.3.1.3 Scope Setup

1. Setup Trigger A Event to Edge, source to chan1,
2. Setup Trigger A-B Event with Acquisition Delay to 4ns.

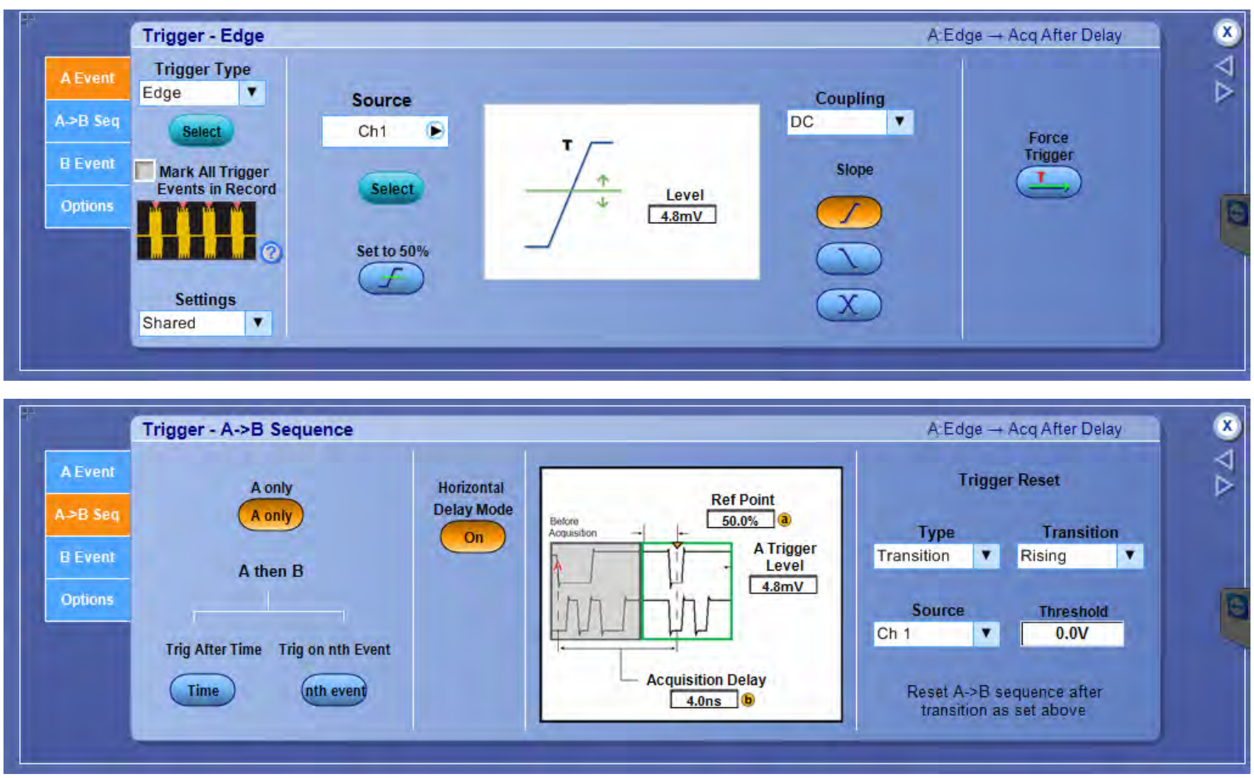


FIGURE 80 SCOPE SETUP

1. Scale Ch1 and Ch2, Math1 (ch1-ch2)
2. Set Acquisition to Average to 2048
3. Acquire the Waveform.
4. Save the Waveform.

FIGURE 81 ACQUIRED WAVEFORM

5. Modify Waveform to Seasim compatible format.

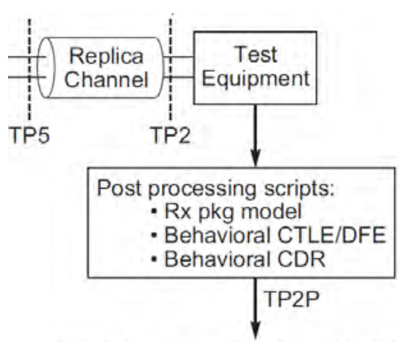


FIGURE 82 APPLY SEASIM

6. Apply the Rx Behavioral Package

   a) Rx Behavioral Package (in S2P/S4P) file.
   b) CTLE /DFE and CDR can be simulated in Seasim.

c) Rx Package model is convoluted externally with Step response before input to Seasim
d) Step response is convert to Frequency domain, then multiply the magnitude with s2p S21 magnitude and phase corresponding to its frequency range.
e) It can be realized using python script.
f) A comparison of original frequency response (red), and the after application of s2p (purple), showing the s2p Rx package s21 graph as a green line.

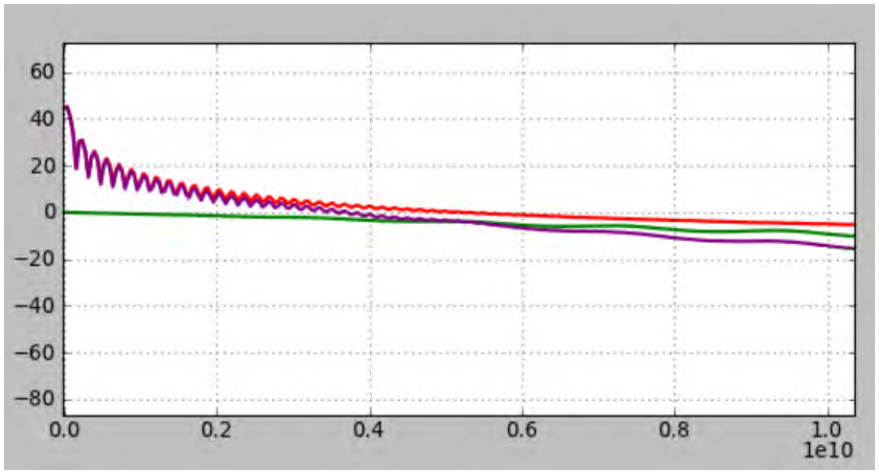


FIGURE 83 GRAPHICAL COMPARISON OF ORIGINAL AND AFTER-APPLICATION RESPONSE

g) Step response before (red) and after (purple).

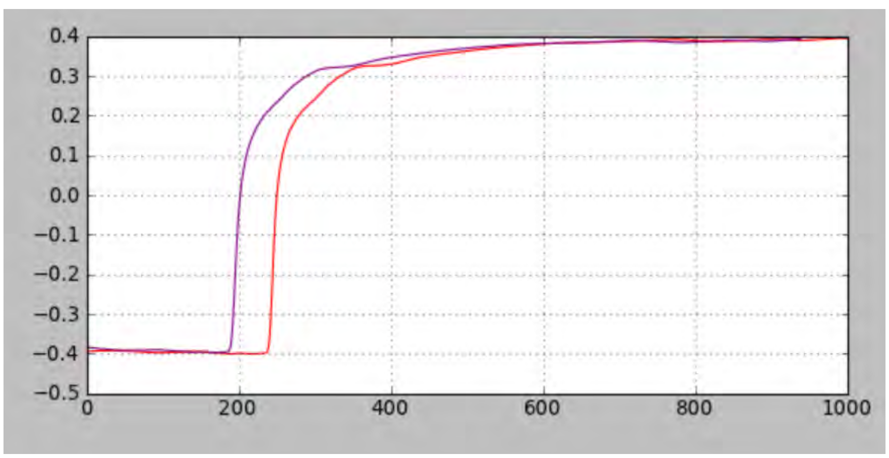


FIGURE 84 GRAPHICAL STEP RESPONSE COMPARISON

7. Run Seasim:

a) Set the Base Name for Step to filename saved.

b) Check the options on top save as picture below.

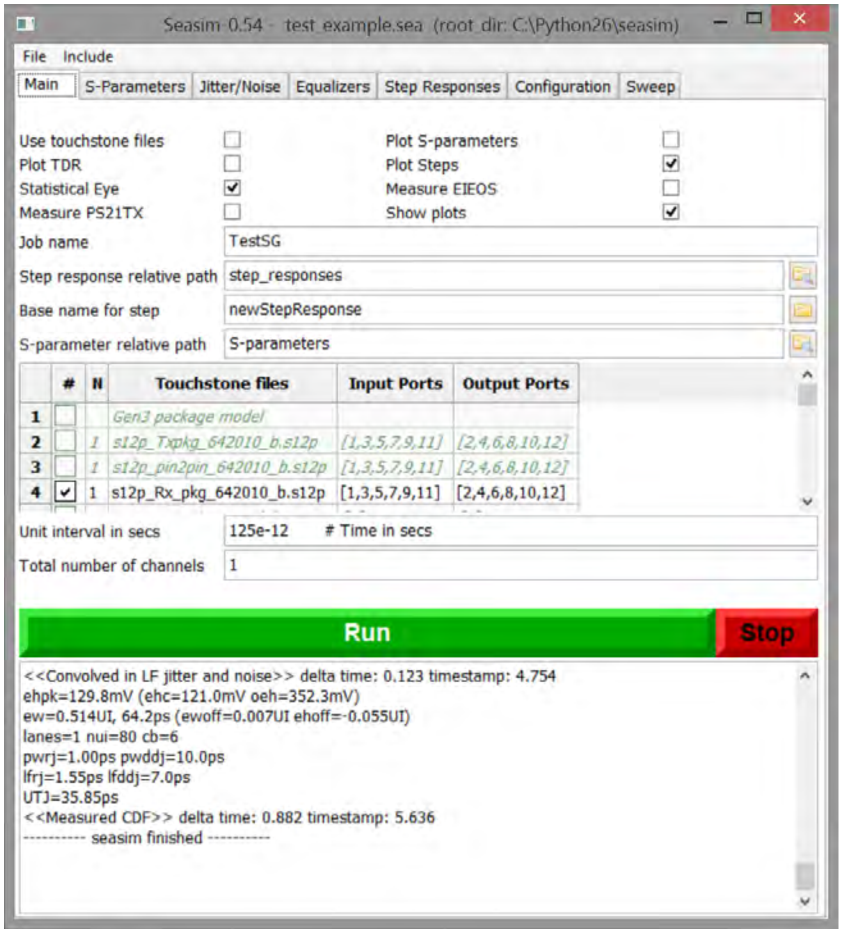


FIGURE 85 SEASIM BASE NAME SETUP

c) On Jitter Noise tab:

i) Set the Corresponding Jitter value for Rj, Sj, DM-SI.
ii) DM-SI value need to tuned and vary to achieve EH.
iii) Set DM-SI to 0mV for start.
iv) Set LF Random Jitter = Rj (2ps).
v) Set LR Uniformly distributed Jitter = Sj (0.1UI).

vi) Set LF Uniformly Distributed Voltage Noise = DM-SI 14mV or more.

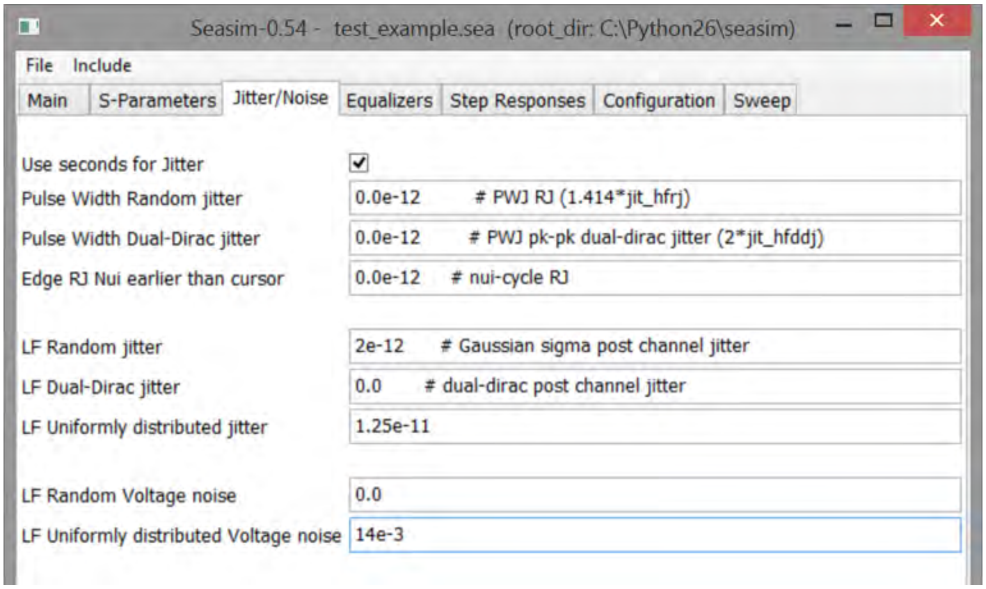


FIGURE 86 SEASIM JITTER/NOISE SETUP

d) On Equalizer tab:

i) Set the DFE taps and max Magnitude.
ii) If Long channel set to [0.000] (Disable DFE)
iii) If Short and None, set to [0.030], Enable with Max of 30mV.

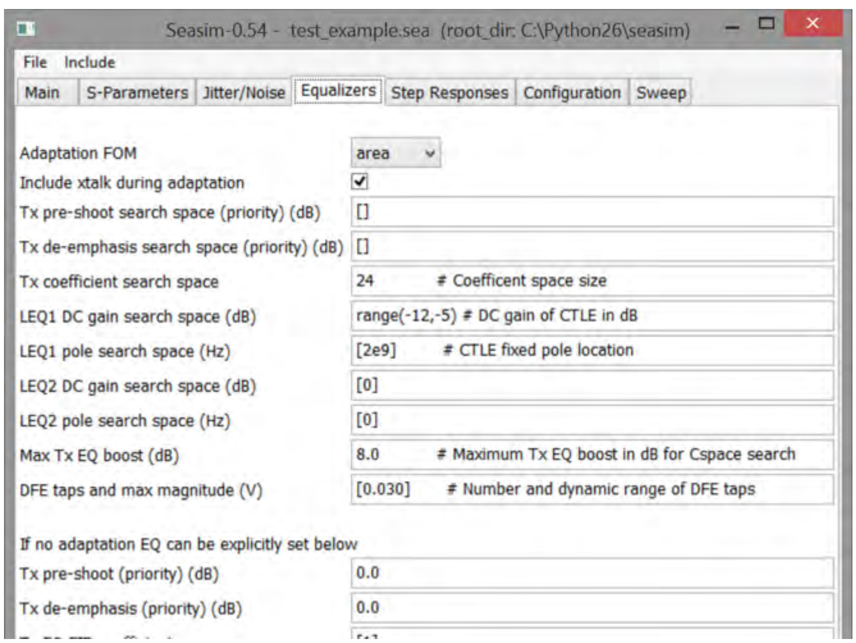


FIGURE 87 SEASIM EQUALIZER SETUP

e) Run Simulation.

8. Simulated Eye Diagram will be created, with its calculated EH and EW at BER-12 based on jitter input.

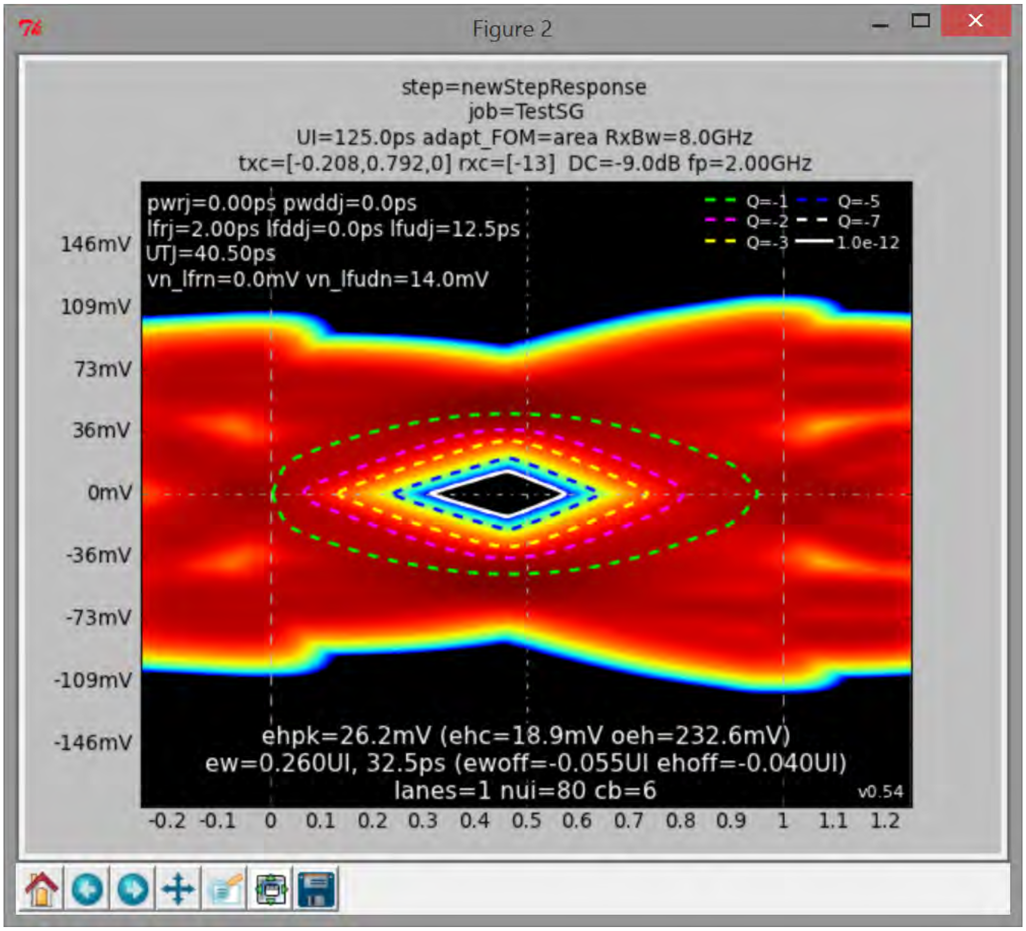


FIGURE 88 SEASIM SIMULATED EYE DIAGRAM #1

9. Observe the EH and EW.

10. Change the DM-SI value to 15mV and run simulation again.

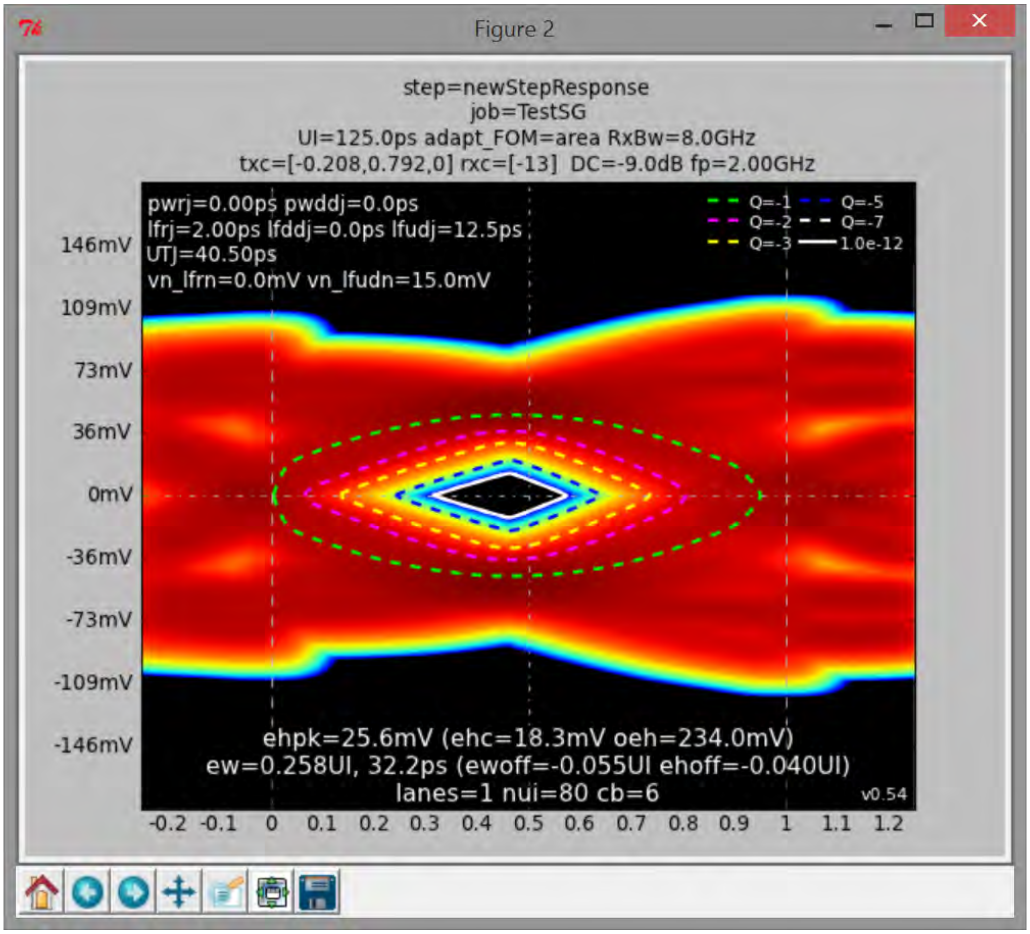


FIGURE 89 SEASIM SIMULATED EYE DIAGRAM #2

11. Change the DM-SI value to 16mV and run simulation again.

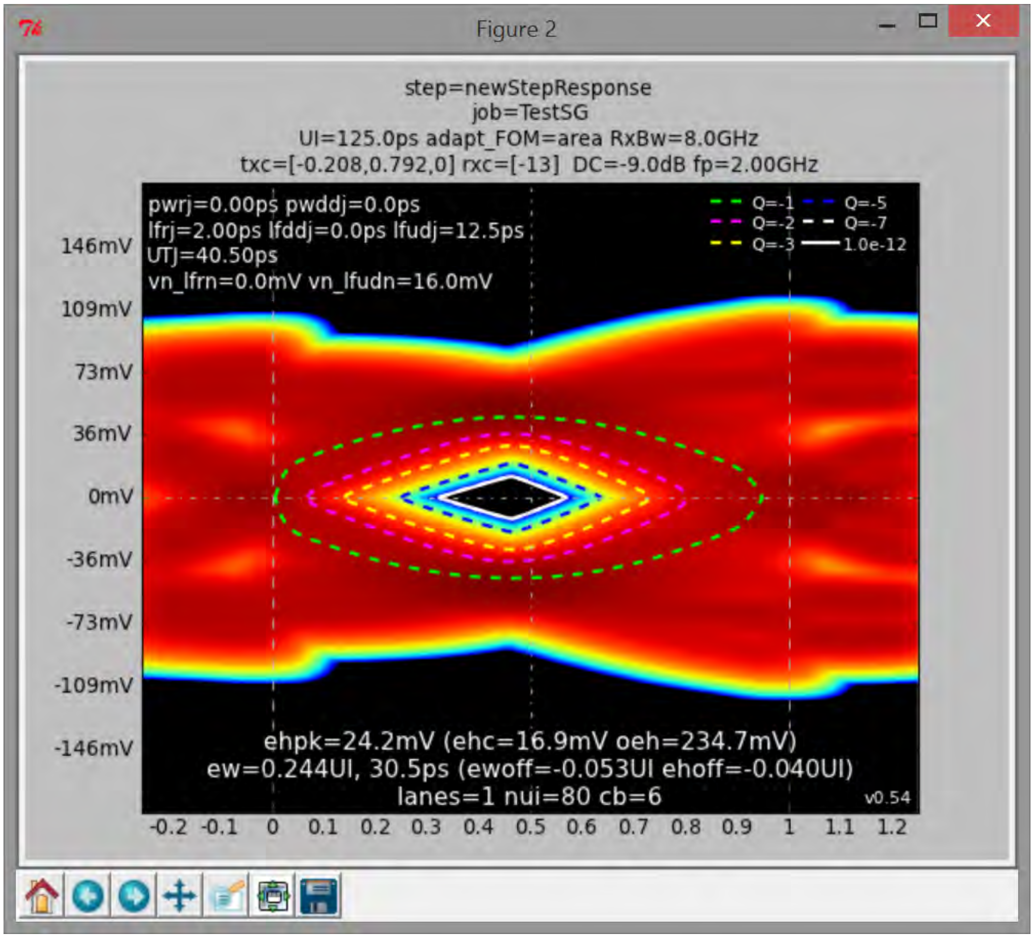


FIGURE 90 SEASIM SIMULATED EYE DIAGRAM #3

12. Calibrate until EH is obtained.

(*) If EW range cannot be achieved, Increase the Amplitude from 800mV to 900mV and perform the Stress Voltage calibration again until EH and EW are obtained.

9.3.2 Stressed Jitter Calibration (For Long Channel Only)

The stressed jitter calibration procedure is similar to that of stressed voltage. Only the long calibration channel (-20 dB) is used. Note that the same post processing scripts are applied identically as they are for the stressed voltage eye case. Eye width is fine-tuned by making adjustments to the Rj source, while EH may be adjusted by varying the launch voltage at the generator.

PCI EXPRESS BASE SPECIFICATION, REV. 3.0

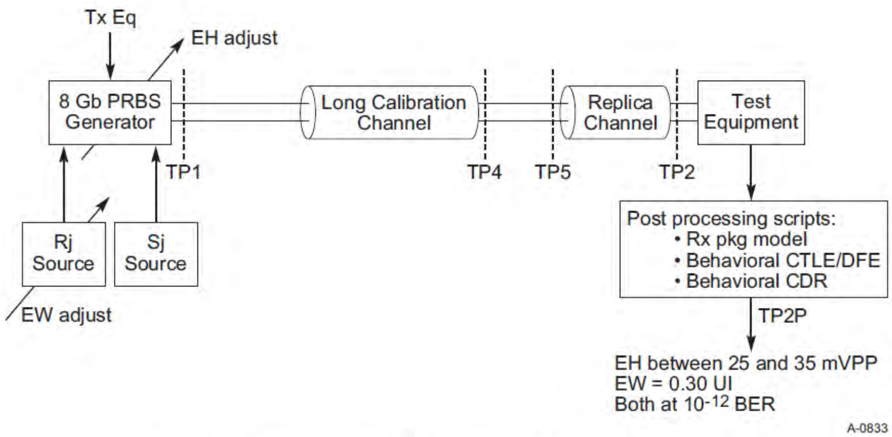


Figure 4-73: Layout for Calibrating the Stressed Jitter Eye

FIGURE 91 LAYOUT FOR LONG CHANNEL CALIBRATION

Table 4-23: Stressed Jitter Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800 (nominal)	mVPP	Measured at TP1, see Figure 4-65. See Note 1.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-ST-8G}$	Eye height at TP2P	25 (min) 35 (max)	mVPP	At BER=10^{-12}. See Note 2.
$T_{RX-ST-8G}$	Eye width at TP2P	0.30	UI	At BER=10^{-12}. See Note 2.
$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 – 1.0	UI PP	See Figure 4-74 Measured at TP1. See Note 3.
$T_{RX-ST-RJ-8G}$	Random Jitter	3.0	ps RMS	Rj spectrally flat before filtering. Measured at TP1. See Note 4.

FIGURE 92 SPECIFICATION FOR LONG CHANNEL CALIBRATION

9.3.2.1 BERTScope Setup

1. Set BERTScope Pattern to clk/256
2. Turn Off Rj, Sj, DM-Si at BERTScope.
3. Set DPP Output to 800mV Amplitude calibrated earlier.
4. Set DPP Deemphasis and Preshoot to Preset 7 for Short channel. Preset 4 for other channel Type.
5. Turn Off AFG.

9.3.2.2 Scope Setup

1. Setup Trigger A Event to Edge, source to chan1,
2. Setup Trigger A-B Event with Acquisition Delay to 4ns.

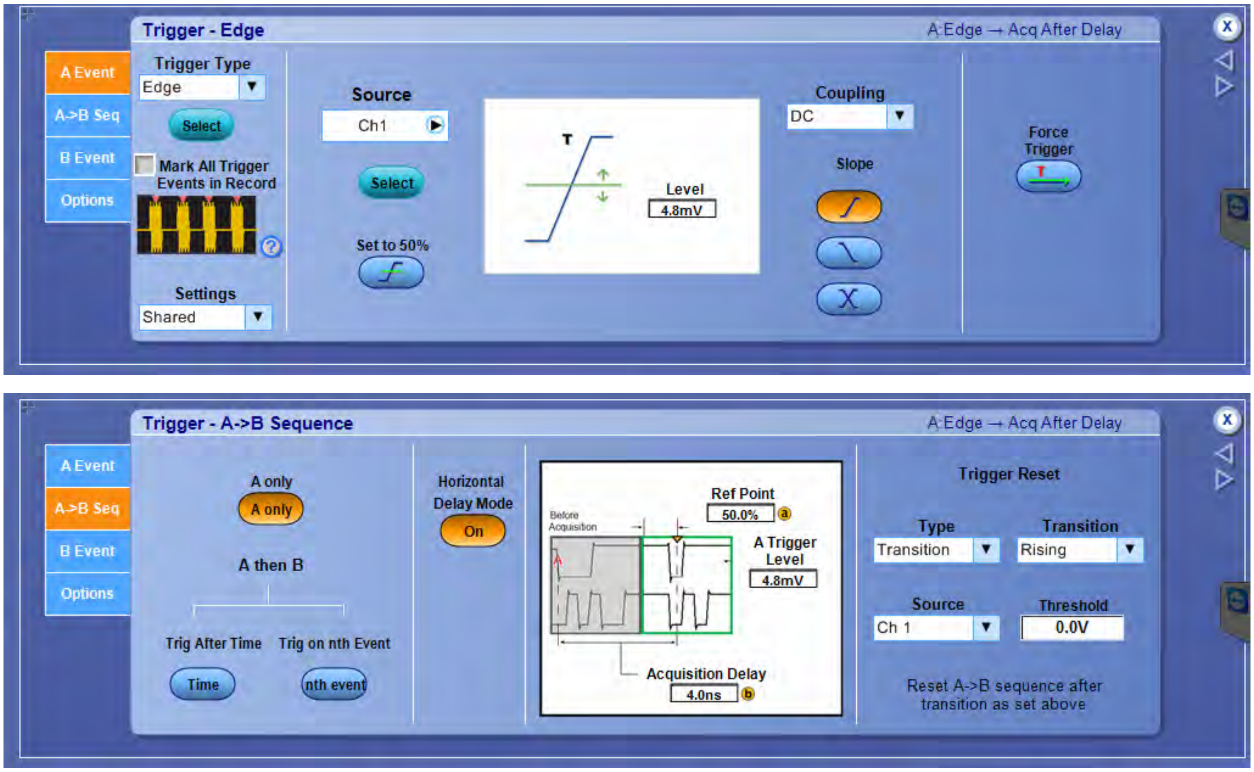


FIGURE 93 SCOPE SETUP

3. Scale Ch1 and Ch2, Math1 (ch1-ch2).
4. Set Acquisition to Average to 2048.
5. Acquire Waveform.
6. Save Waveform.
7. Modify Waveform to Seasim compatible format.

9.3.2.3 Apply Rx Behavioral Package

1. Run Seasim:
   a) Set the Base Name for Step to filename saved.
   b) Check the options on top save, as shown in Figure 94.

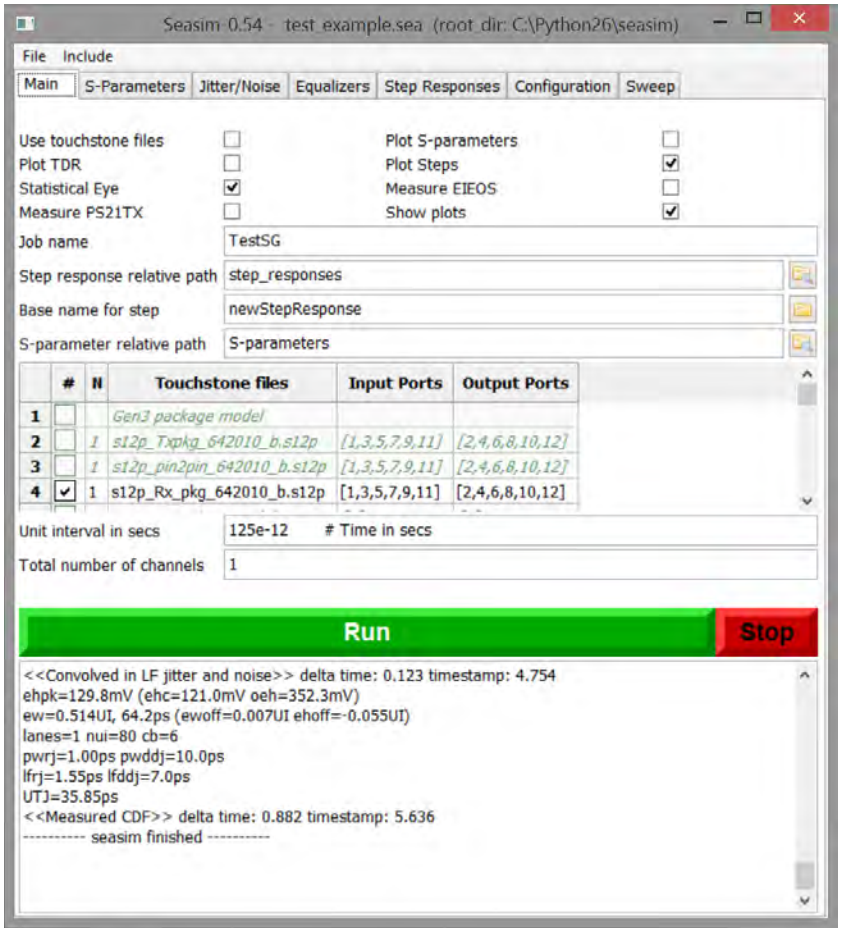


FIGURE 94 SEASIM MAIN SETUP

c) On Jitter Noise tab.

i) Set the Corresponding Jitter value for Rj, Sj.
ii) Rj value need to tuned and vary to achieve EW.
iii) Set LF Random Jitter = Rj (3ps or more).
iv) Set LR Uniformly distributed Jitter = Sj (0.1UI).
v) Set LF Uniformly Distributed Voltage Noise = 0.0mV.

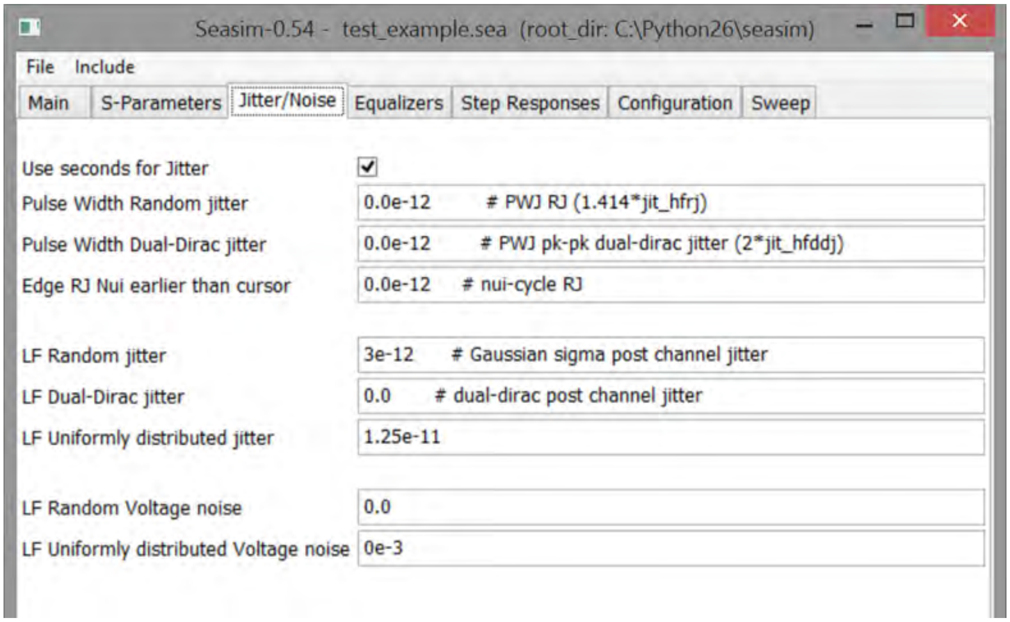


FIGURE 95 SEASIM JITTER/NOISE SETUP

d) Equalizer tab:

i) Set the DFE taps and max Magnitude.

ii) Set to [0.030].

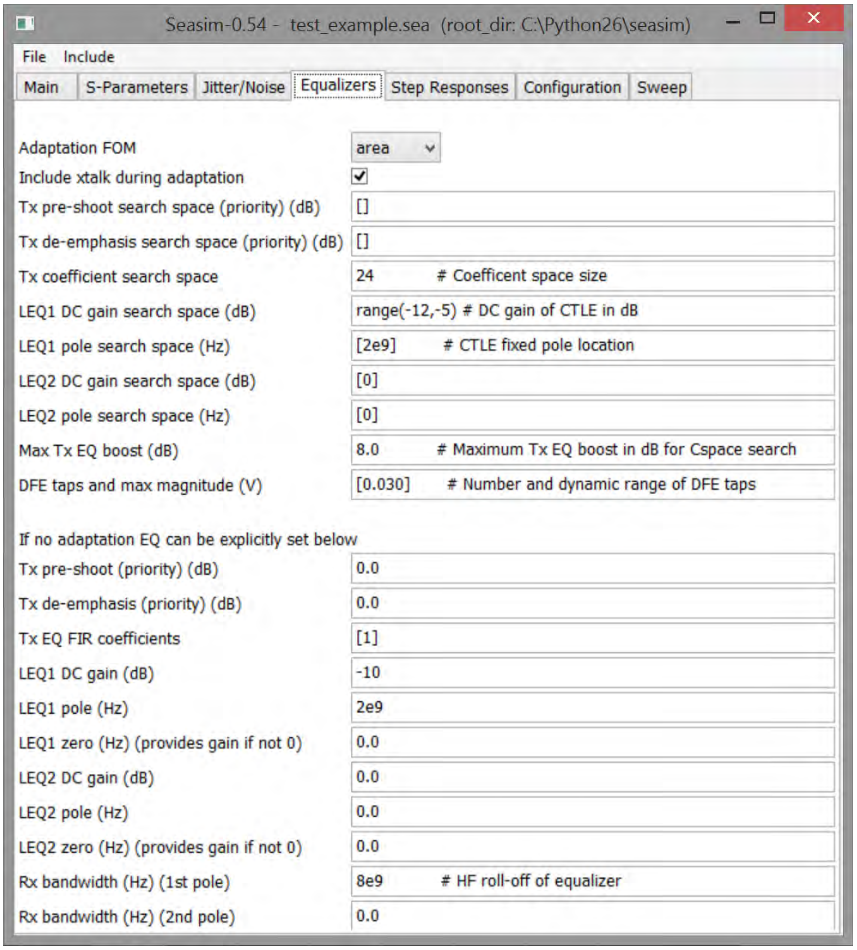


FIGURE 96 SEASIM EQUALIZER SETUP

e) Run Simulation.

2. Simulated Eye Diagram will be created with its calculated EH and EW at BER-12 based on jitter input.

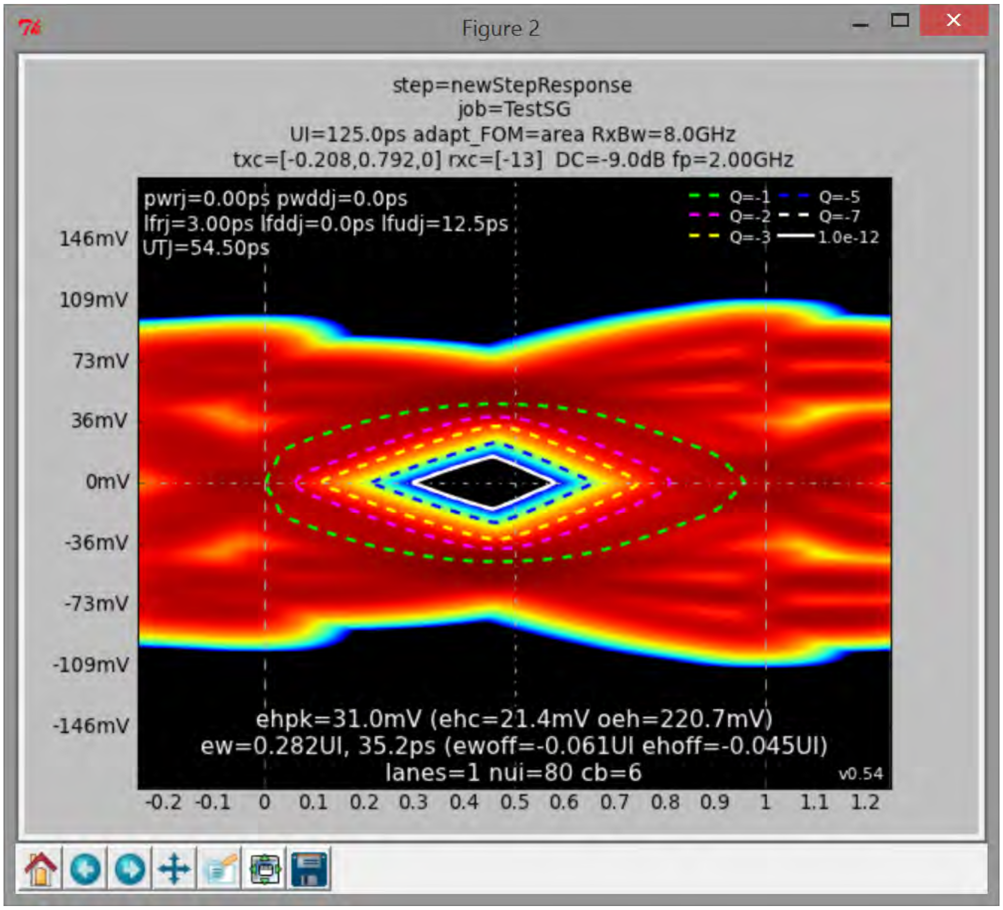


FIGURE 97 WAVEFORM #1

3. Observe the EH and EW.
4. Change the Rj value and run simulation again.
5. Calibrate until EW is obtained.

(*) If EH range cannot be achieved, Increase the Amplitude from 800mV to 900mV and perform the Stress Jitter calibration again until EH and EW are obtained.

9.4 Receiver Test

9.4.1 Equipment Setup

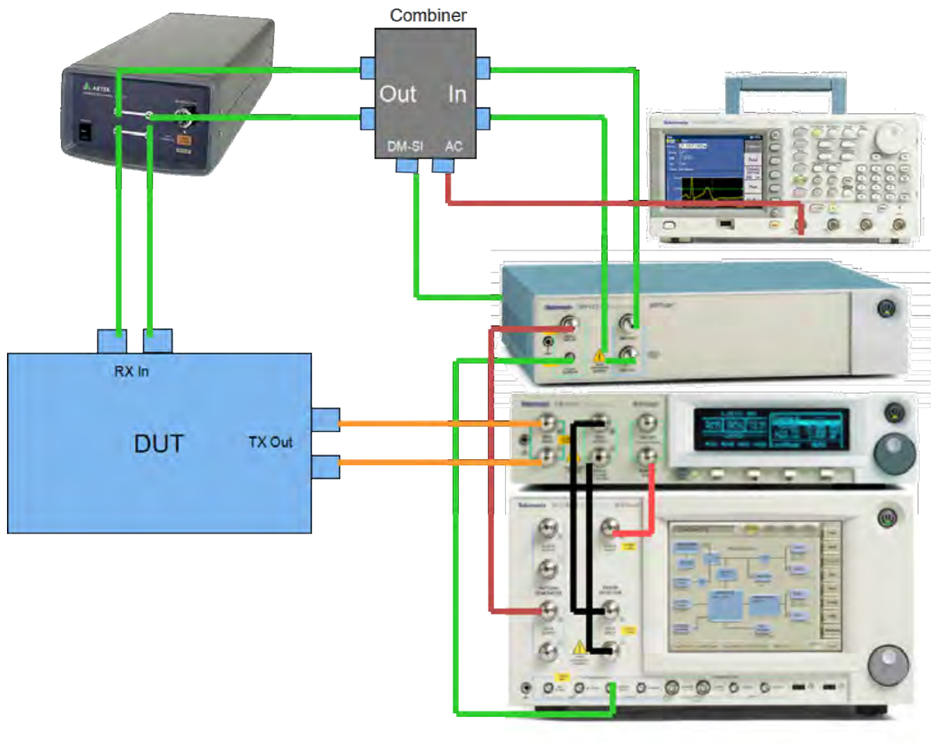


FIGURE 98 RECEIVER TEST EQUIPMENT SETUP

9.4.1.1 Connection Steps

1. Connect BERTScope Data(+) to DPP.
2. Connect BERTScope Clk Out to DPP.
3. Connect DPP Data(+) out to Combiner In.
4. Connect DPP Data(-) out to Combiner In.
5. Connect AFG Output1 to Combiner CM-IN.
6. Connect BERTScope (real panel) SI-out to Combiner DM In.
7. Connect Combiner Data Out to Artek Box.
8. Connect Artek Box Out to DUT In.
9. Connect DUT Tx Out to Clock Recovery CR125A Data In.
10. Connect CR125A Data out to BERTScope Detector Data In.
11. Connect CR125A Subrate Clock Out to BERTScope Detector Clock In.
12. Connect the External Clock from BERTScope to DUT as Ref Clk (100MHz).

9.4.2 Stressed Voltage Receiver Test

Once a calibrated EH and EW have been obtained, the cables are moved to connect the Rx DUT to the far end of calibration channel. The Tx equalization is then optimized as it was for the stressed voltage eye with the assumption that the DUT Rx will also optimize its equalization. Sj is set to an initial value that permits the receiver CDR to achieve lock.

9.4.2.1 Configure BERTScope

1. Set Generator to 8Gpbs.
2. Set the Pattern to PCIe_8G_BruteFor.RAM.

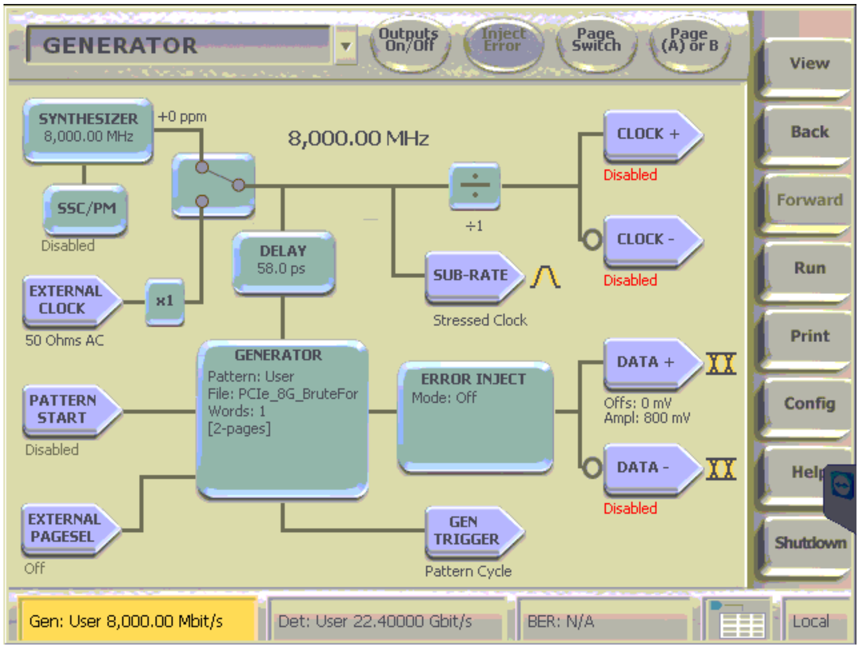


FIGURE 99 RECEIVER TEST CONFIGURE BERTSCOPE

9.4.2.2 Configure for Stressed Jitter

1. Set the Calibrated SJ for 0.1UI at 100MHz.
2. Set the Calibrated Rj for 2ps(RMS).
3. Set the Calibrated Sine Interference Amplitude that is calibrated to achieve EH and EW (DM-SI).
4. Set the Sine Interference Frequency to 2.1GHz.
5. Set the Sine Interference mode to External.
6. Set the DPP Output to calibrated amplitude to achieve EH and EW.

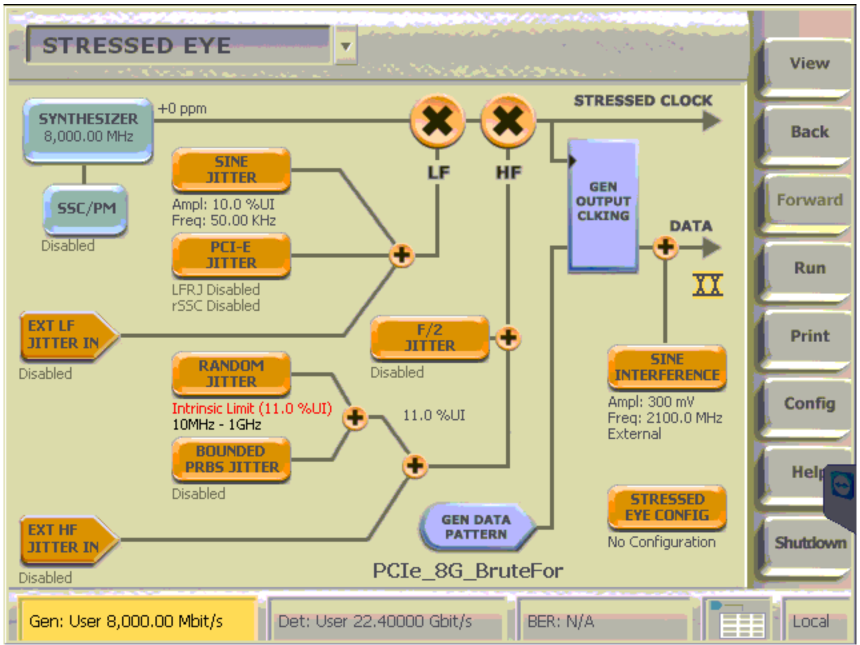


FIGURE 100 RECEIVER TEST CONFIGURE FOR STRESSED JITTER

7. Configure ISI by setting Artek ISI % value to calibrated channel Type.
8. Configure AFG:
   a) Set Output1 of AFG ON
   b) Set Output1 Mode to Sine Wave
   c) Set Sine Wave Frequency to 120MHz
   d) Set the Sine Wave Amplitude to Calibrated value.
9. Setup the BERTScope Detector:
   a) Click the Auto Align

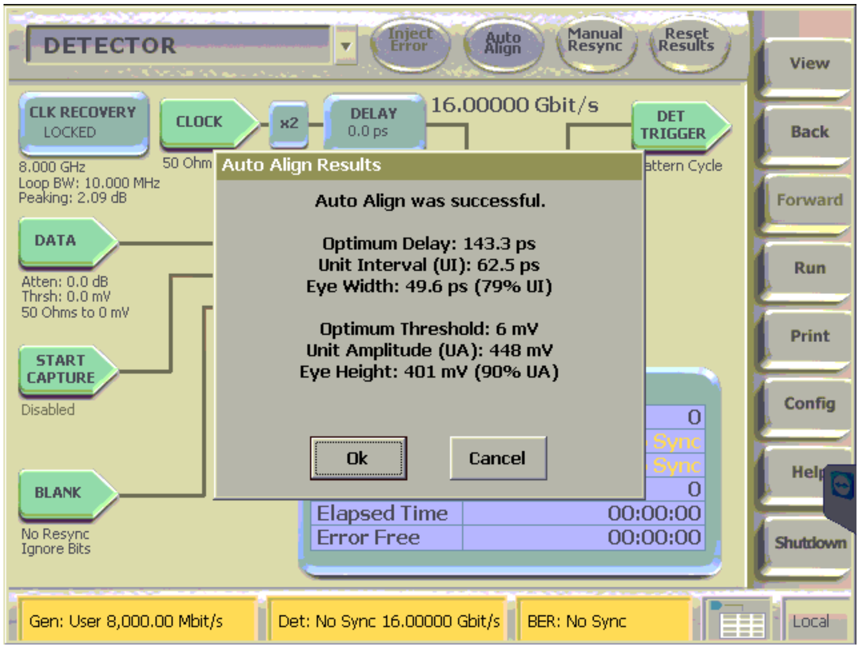


FIGURE 101 RECEIVER TEST CONFIGURE BERTSCOPE DETECTOR

9.4.2.3 Bit Error Rate Test

1. With the DUT in loopback mode, and BERTScope synchronize with pattern.
2. Compliance test may begin.
3. Click the Reset Result.
4. Click the RUN.
5. Let the Detector Run, stop when the BITs is more than 1xE12.
6. Read the Error value.
7. If the error is zero (0), then the test passes.

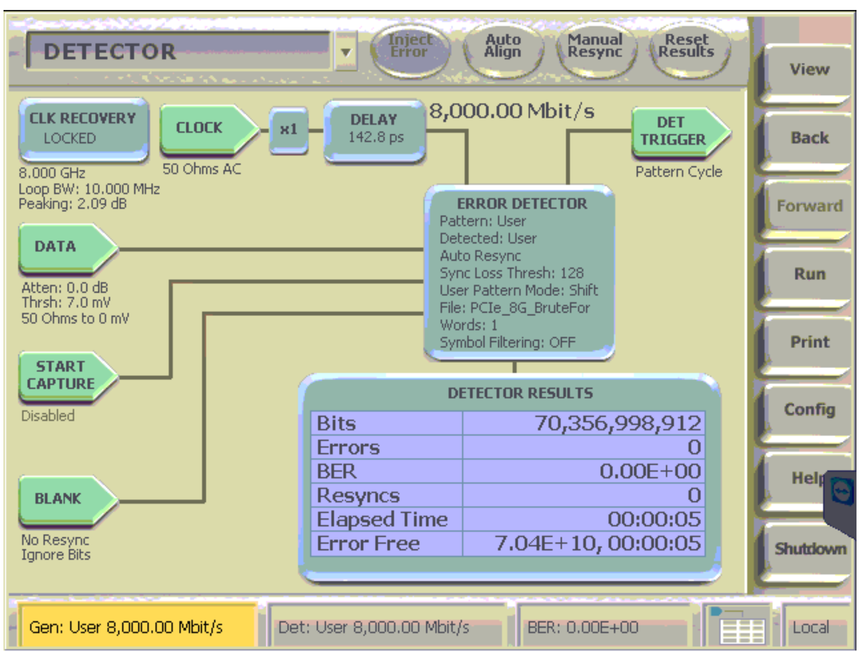


FIGURE 102 RECEIVER TEST PERFORM BER TEST

9.4.3 Stressed Jitter Receiver Test (100MHz)

9.4.3.1 Configure BERTScope

1. Set Generator to 8Gpbs.
2. Set the Pattern to PCIe_8G_BruteFor.RAM.

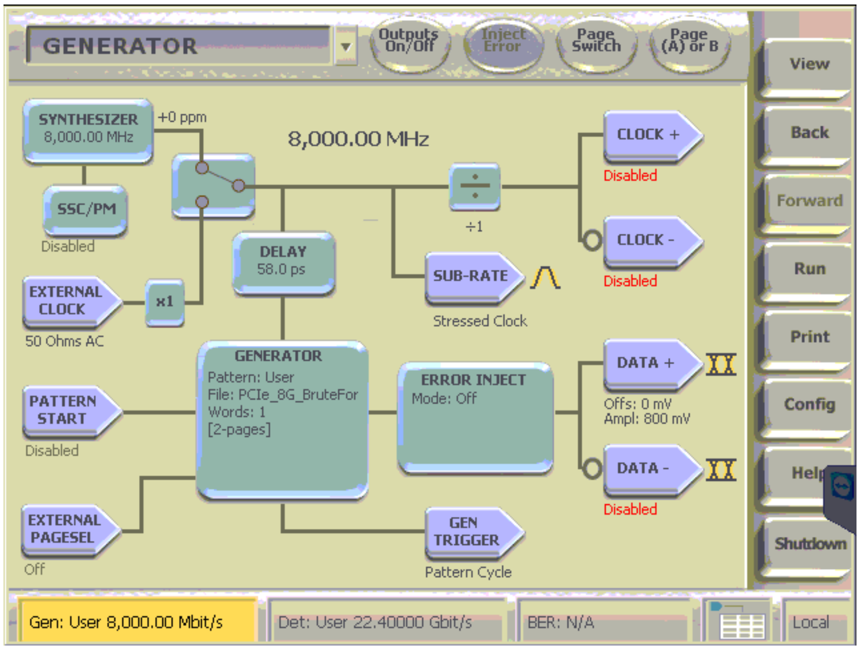


FIGURE 103 RECEIVER STRESSED JITTER TEST BERTSCOPE SETUP

9.4.3.2 Configure for Stressed Jitter at 100MHz

1. Set the Calibrated SJ for 0.1UI at 100MHz.
2. Set the Calibrated RJ that is calibrated during Stressed Jitter Calibration that achieved EW and EH.
3. Set the Calibrated Sine Interference to 0mV.
4. Set the DPP Output to calibrated amplitude to achieve EH and EW.

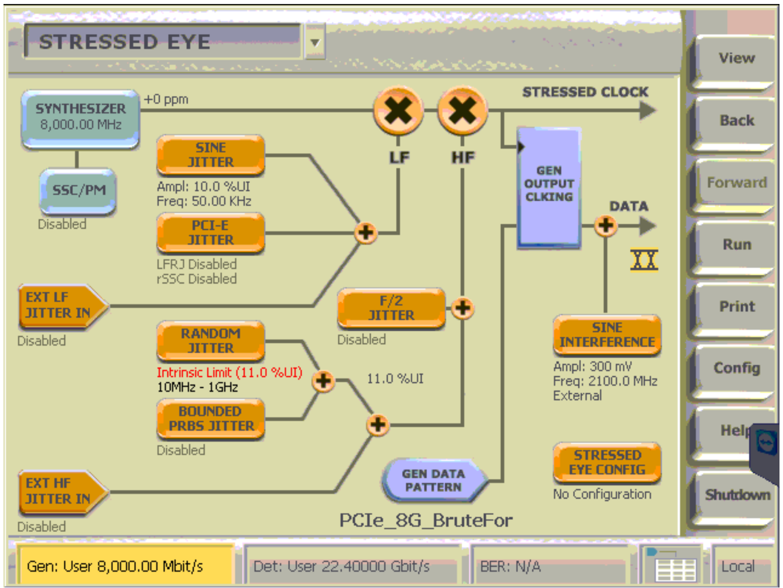


FIGURE 104 RECEIVER STRESSED JITTER TEST BERTSCOPE SETUP

5. Configure ISI by setting Artek ISI % value to calibrated channel Type.
6. Configure AFG by setting Output1 of AFG OF.
7. Setup the BERTScope Detector by clicking on Auto Align.

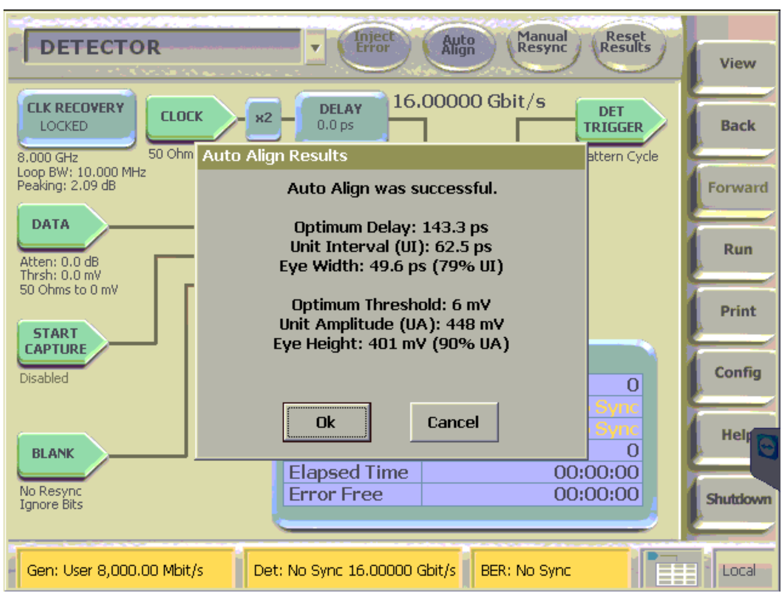


FIGURE 105 RECEIVER STRESSED JITTER TEST BERTSCOPE DETECTOR

9.4.3.3 Bit Error Rate Test

1. With the DUT in loopback mode, and BERTScope synchronize with pattern.
2. Compliance test may begin.
3. Click the Reset Result.
4. Click the RUN.
5. Let the Detector Run, stop when the BITs is more than 1xE12.
6. Read the Error value.
7. It is Pass if error is 0.

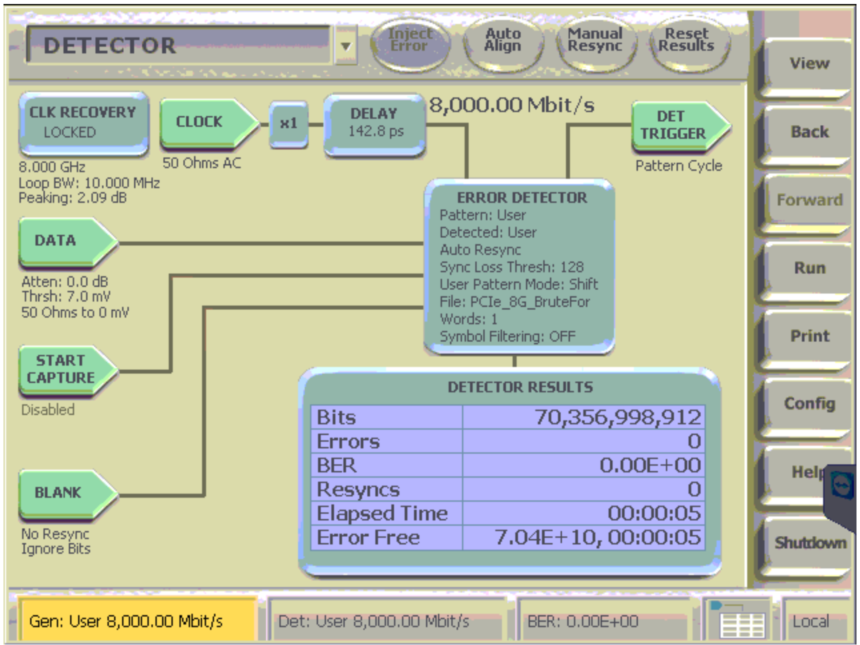


FIGURE 106 RECEIVER STRESSED JITTER PERFORM BER TEST

10 PVT Automation

Granite River provides software to support repeated testing within sequences of parameter values, which are applied to the DUT during the tests.

10.1 Available Parameters

Table 5 lists the parameters which can be controlled by the PVT Automation software. Up to eight values may be specified for each parameter.

TABLE 5. AVAILABLE PARAMETERS

Symbol	Parameter	Units
RJ	Random Jitter	Picoseconds
ISI	Inter Symbol Interference	Per cent of UI
SJ	Sinusoidal Jitter	Picoseconds
Amplitude	Launch Voltage	Millivolts, peak-to-peak
CM	Common Mode (noise source)	
DM	Differential Mode (noise source)	

10.2 Applicable Tests

Table 6 lists the tests which can be controlled by the PVT Automation software. PVT parameters have no effect on other tests in the suite.

TABLE 6. APPLICABLE TESTS

Test Title
Stress Voltage Sweep Test (none)
Stress Voltage Sweep Test (short)
Stress Voltage Sweep Test (long)
Stress Jitter Sweep Test (long)

10.3 Setting up PVT Value Sequences

1. Select the PVT Configuration icon on the toolbar. See Figure 107.

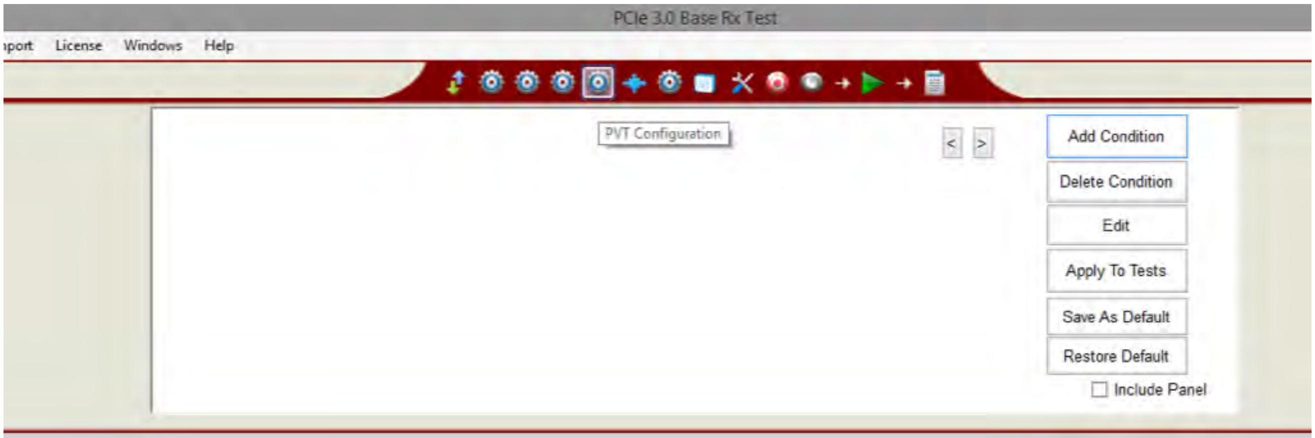


FIGURE 107 SELECT PVT CONFIGURATION

2. Add a parameter to the selected test by selecting "Add Condition". See Figure 108, which selects 'SJ' as the new condition group. No drop-down menu of allowed parameter names is provided. Refer to Table 5. A short description may be provided. This description, and the names of the individual step 'Variables' are all included in the test results Report.

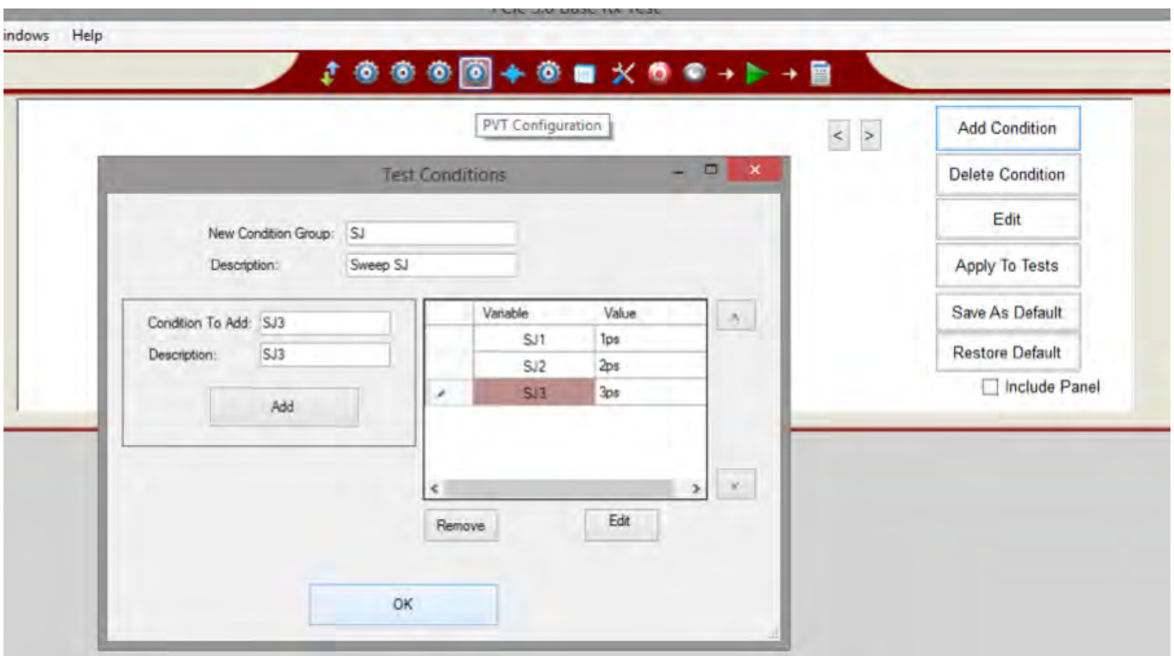


FIGURE 108 ADD FIRST PVT AUTOMATION PARAMETER

3. Enter one or more parameter value for the steps of the test condition sequence. Take care to include the suffix for the units, and to assign values which are appropriate for that parameter according to the PCIE3 specification. See Figure 109, which shows four steps for parameter 'SJ', named 'SJ1', 'SJ2', 'SJ3' and 'SJ4', and assigned values 1ps, 1.2ps, 1.8ps and 3ps, respectively. When finished editing the Test Conditions, click on "OK". Note that individual steps may be selected, then edited or removed from the list.

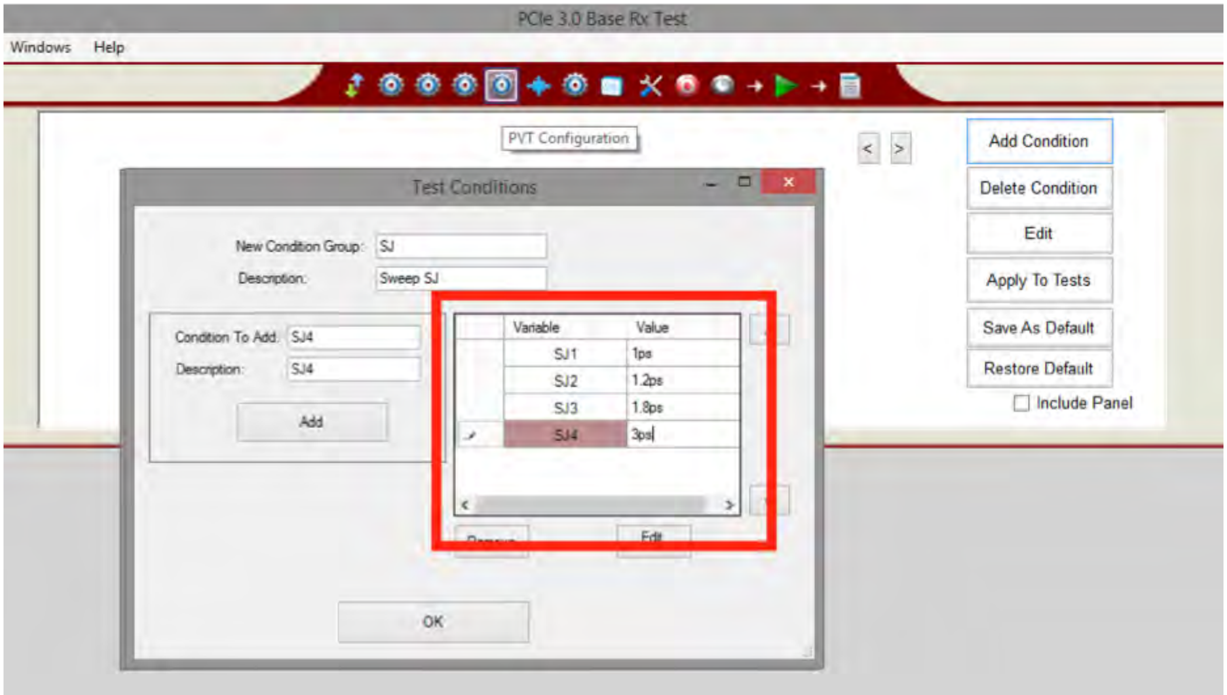


FIGURE 109 SET EACH PVT PARAMETER VALUE IN SEQUENCE

4. Add a second parameter. See Figure 110., which adds 'SweepISI', with three values, each expressed as a percentage.

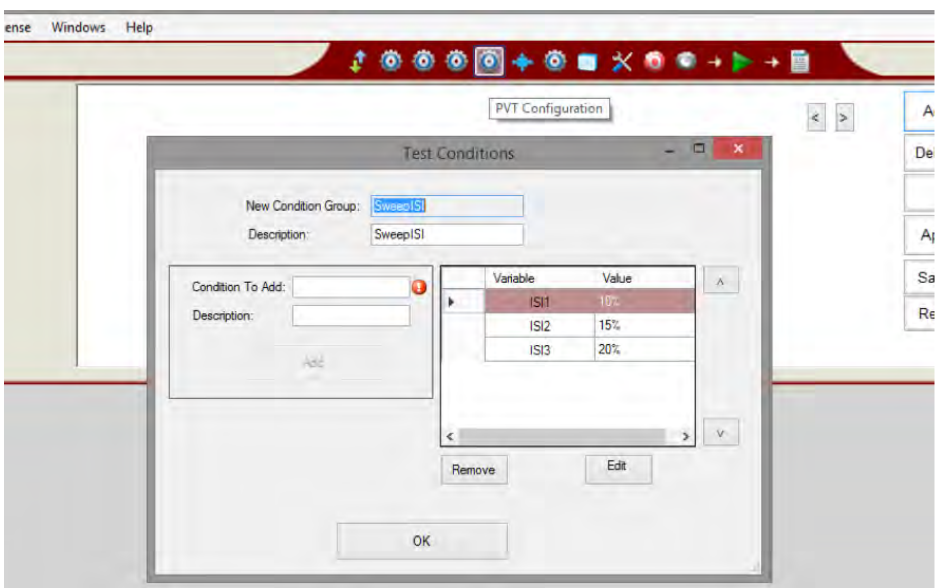


FIGURE 110 ADD SECOND PVT PARAMETER

5. Repeat setting values to each of the allowed parameters. Those parameters which are not setup with explicit values will use the default value.

6. From the menu, apply the sequences of parameters to the selected tests (see Figure 111 and Figure 112), which builds a "Stress Test Plan".

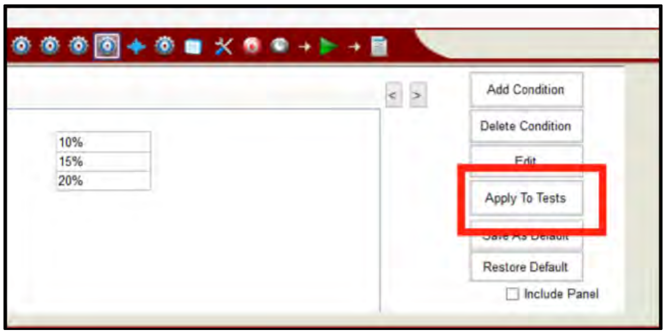


FIGURE 111 APPLY TO TESTS

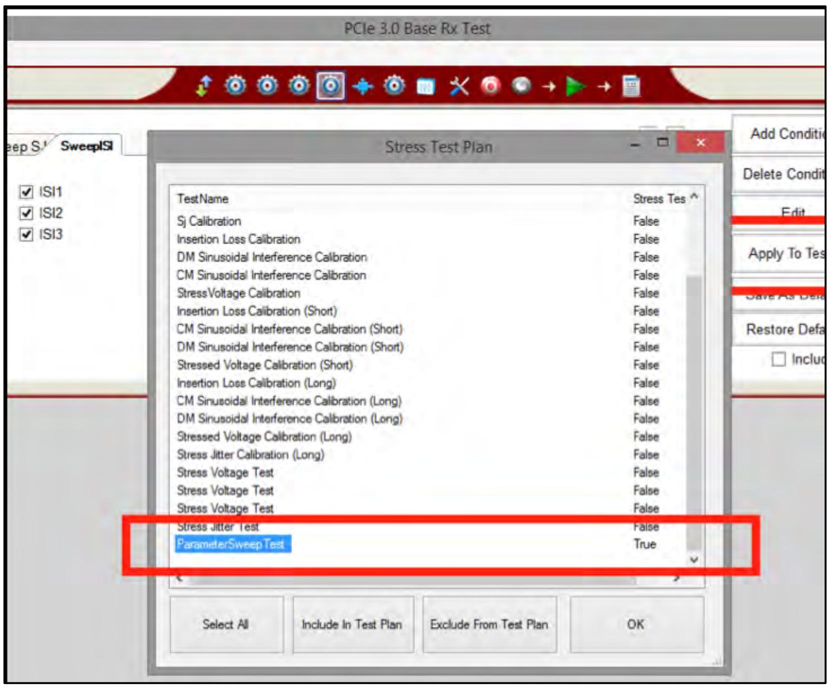


FIGURE 112 SELECT APPLICABLE TESTS

7. Select the PVT tests to run (see Figure 113).

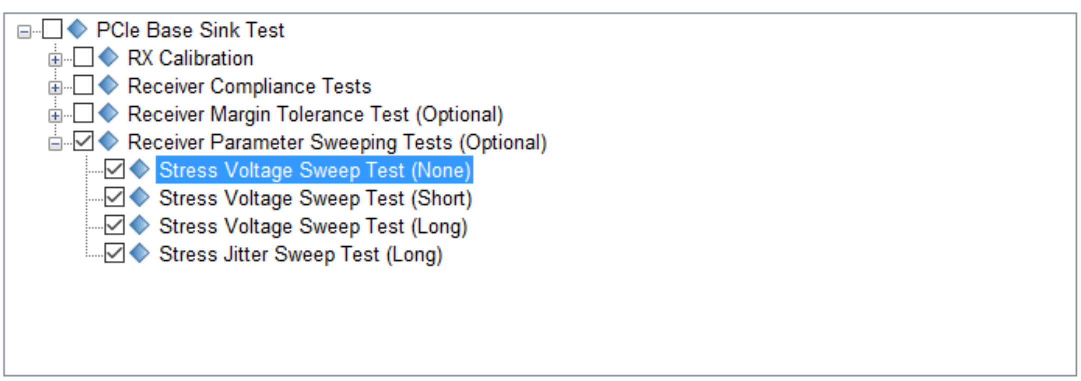


FIGURE 113. SELECT PVT TESTS TO RUN

8. Run the tests using the “Run Tests with PVT” button (see Figure 114).

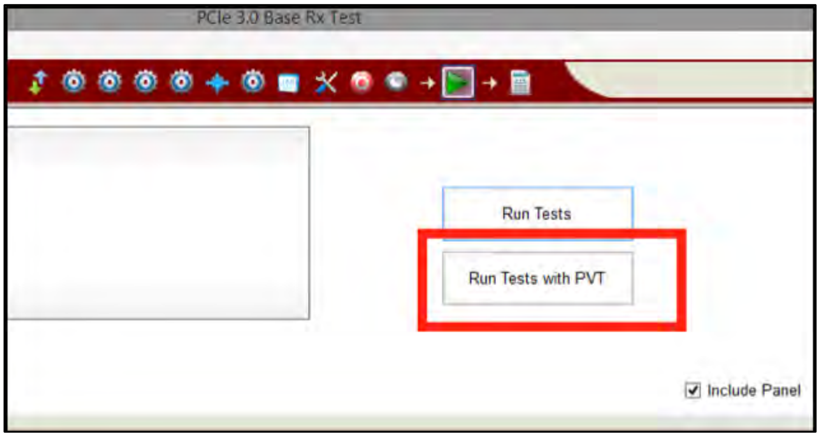


FIGURE 114 RUN TESTS WITH PVT

10.4 Search Algorithm

10.4.1 Jitter Margin Testing

After selecting the parameters and their ranges, the user may select from a list of search algorithms to find the bounds of jitter margin.

TABLE 7. PVT AUTOMATION – INTERNAL JITTER MARGIN SEARCH ALGORITHMS

Symbol	Algorithm
	Bottom-Up
	Top-Down
	Binary

10.5 Test Results

Results from the selected PVT tests, each using the one or more defined PVT parameters, are collected in the Test Report.

The selected tests are all run, one after the other, for each permutation of the parameters. The parameter defined first is varied most slowly; the last-defined parameter is defined most quickly.

For example, considering the parameters and tests defined and selected in Figure 108 to Figure 113 will iterate as shown in Table 8. (Individual parameter step names are not shown.)

TABLE 8. PVT AUTOMATION – ITERATION SEQUENCE EXAMPLE

Seq.	SJ	ISI	Tests
1	1.0ps	10%	All 4 Parameter Sweeping Tests
2	1.2ps	15%	All 4 Parameter Sweeping Tests
3	1.8ps	20%	All 4 Parameter Sweeping Tests
4	3.0ps	10%	All 4 Parameter Sweeping Tests
5	1.0ps	15%	All 4 Parameter Sweeping Tests
6	1.2ps	20%	All 4 Parameter Sweeping Tests
7	1.8ps	10%	All 4 Parameter Sweeping Tests
8	3.0ps	15%	All 4 Parameter Sweeping Tests
9	1.0ps	20%	All 4 Parameter Sweeping Tests
10	1.2ps	10%	All 4 Parameter Sweeping Tests
11	1.8ps	15%	All 4 Parameter Sweeping Tests
12	3.0ps	20%	All 4 Parameter Sweeping Tests

10.6 Saving and Loading a PVT Session

When using the PVT Automation software, the "Save As" and "Restore" buttons are not used. To save a session, with all of the PVT parameter information, the test results, and any waveforms, use the "Options" command on the menu bar, then the "Save Session" command.

To load a session back into the software, including the saved parameter settings, use the "Options" command on the menu bar, then the "Load Session" command.

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

END_OF_DOCUMENT